

Service Manual

LCD TV DVD COMBO

Model: DSL-19M1TC

✓ **Caution**

: In this Manual, some parts can be changed for improving, their performance without notice in the parts list. So, if you need the latest parts information, please refer to PPL(Parts Price List) in Service Information Center

DSL19M1TC SERVICE MANUAL

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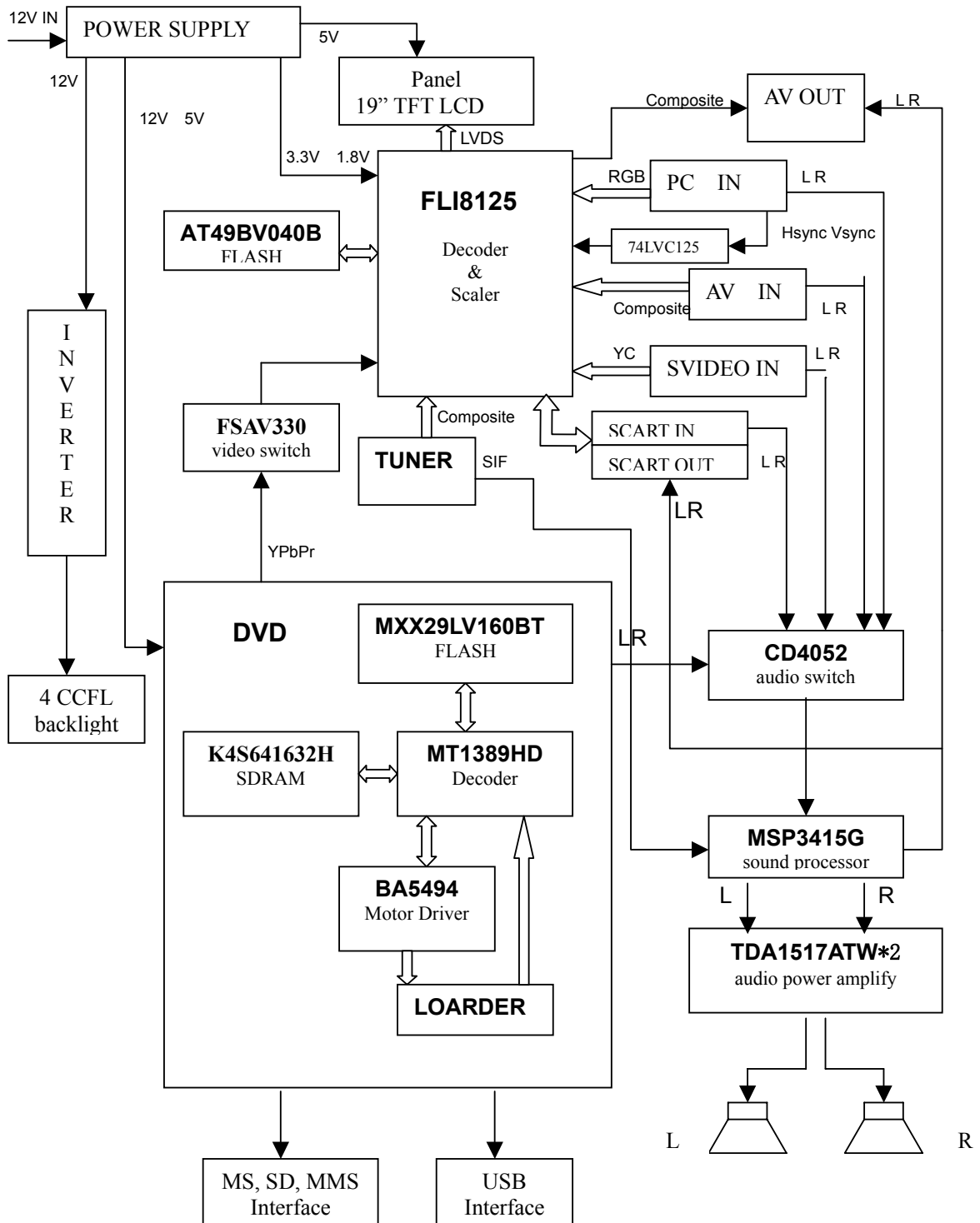
Part 1 Brief Introduction Of The DSL19M1TC

Specification

Thank you for buying ALBA LCD-TV Product. As a high-resolution LCD-TV with a 19-inch screen, the DSL19M1TC incorporates DVD player, LCD display and TV receiver in one system. It adopts an MPEG2 decoding format to achieve horizontal resolution more than 500 lines. Designed with USB and SD/MS/MMC card port, it can be connected to USB device or SD/MS/MMC Card. It has several special functions such as sleep time setting, V-Chip and CCD support, auto TV searching and the picture enlargement. The product can not only be connected to external audio and video signal source and PC, but also features an AV output to external audio and video device. It also supports multi-angle, multi-language and multi-subtitle playback.

Specifications	
Brand	ALBA DSL19M1TC
TV Type	TV With LCD Screen
Dimension	
Depth	184mm
Height	412mm
Width	494mm
Weight	About 8.26 kg
General	
Exterior Color	Black and Silver
Screen Size	19 in.
TFT-LCD Resolution	1440 x 900
Video Inputs	AV, S-Video, Component, VGA, TV, DVD
Video Outputs	Composite
Audio Inputs	L/R audio input (AV audio inputs share with S-Video and Component), PC audio input
Video system	NTSC
Number of Discs	1
Discs Formats	DVD, CD, JPEG
Ambient Temperature	10~45℃
Power Supply	AC 100-240V 50/60 Hz DC 12V 5A
Power Consumption	<60W

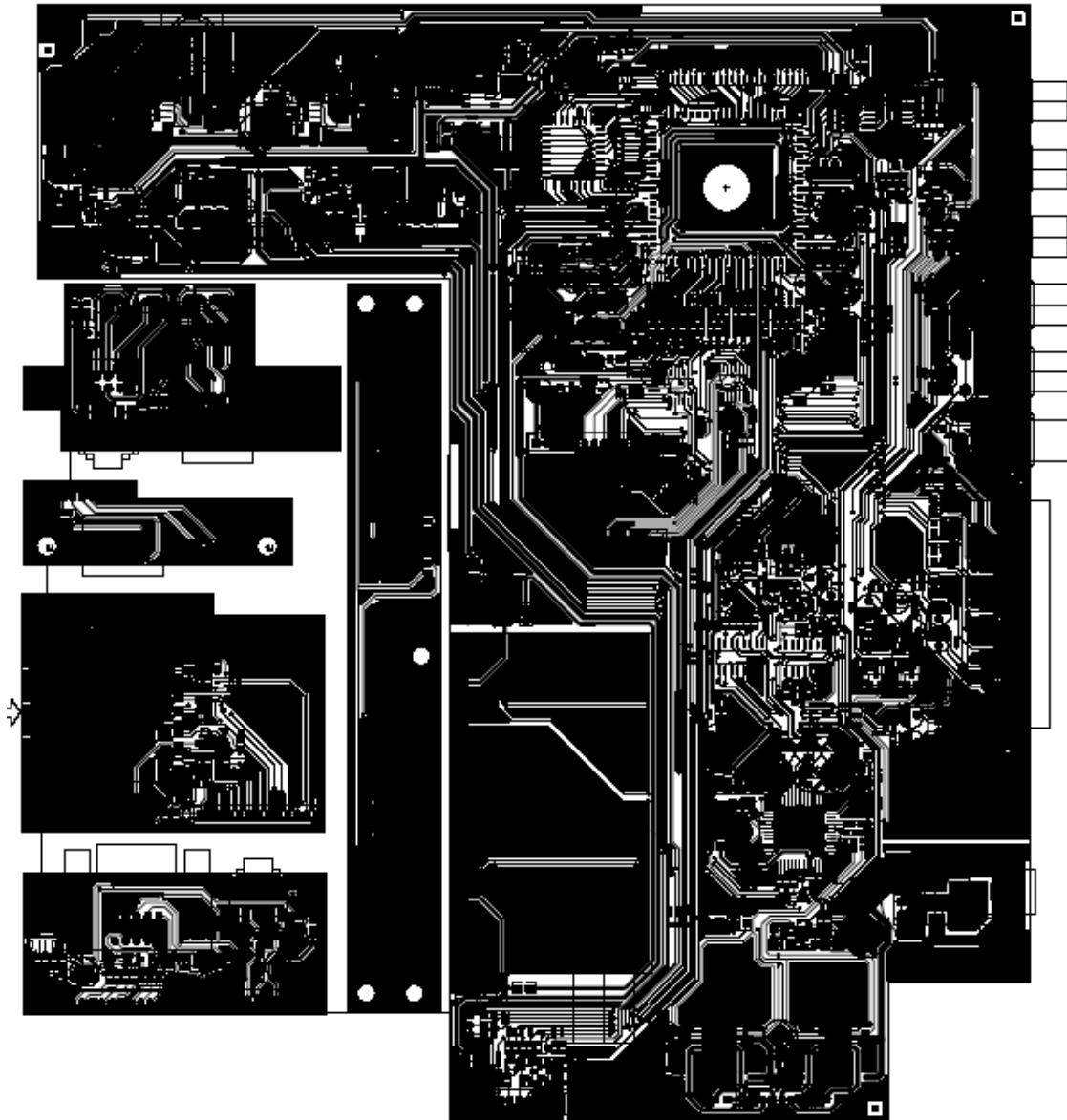
Schematic Diagram



Printed Circuit

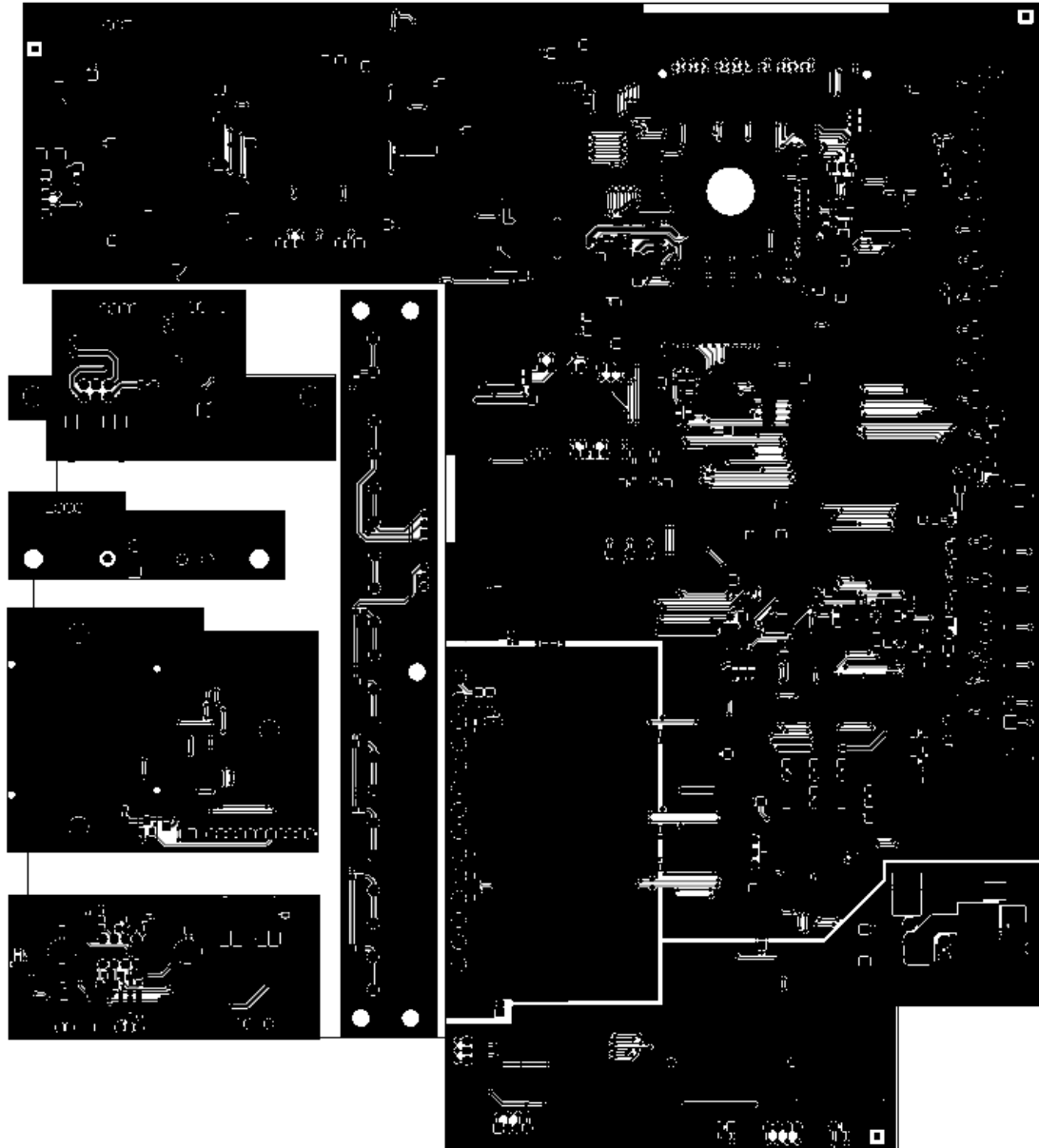
Main Board 3269C SDcard board 3274C Earphone board 3272C
Keystroke board 3270C Remote control board 3271C VGA board 3273C

(Top layer view)

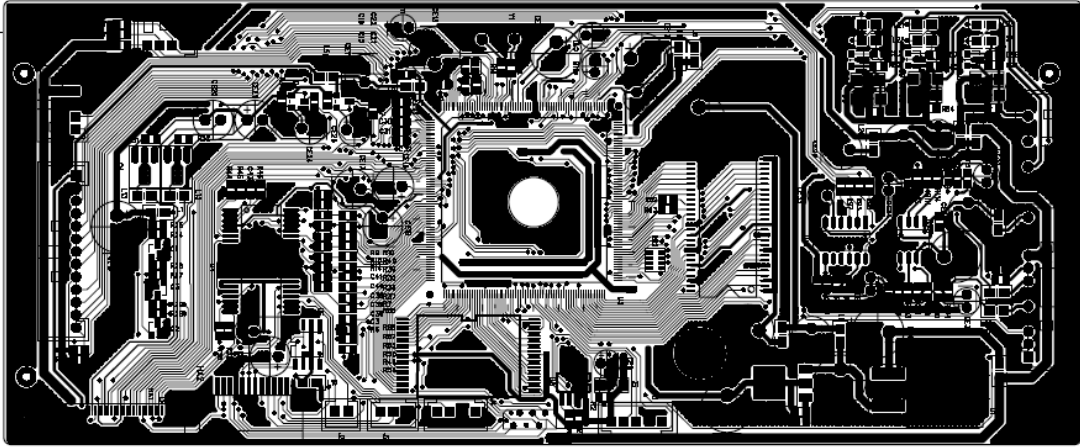


Main Board 3269C SDCard board 3274C Earphone board 3272C
Keystroke board 3270C Remote control board 3271C VGA board 3273C

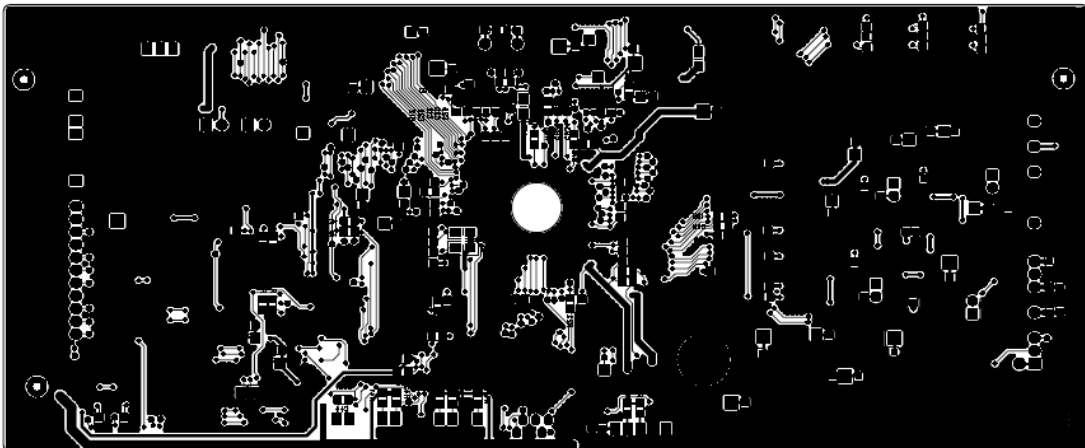
(Bottom layer view)



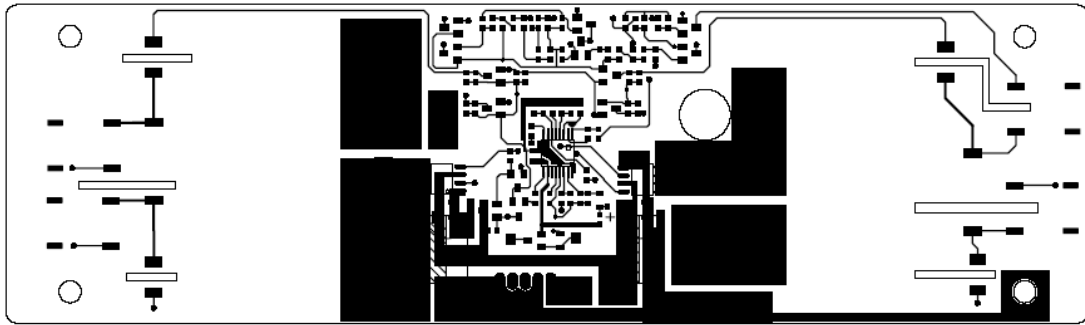
DVD board 2777C(Top layer view)



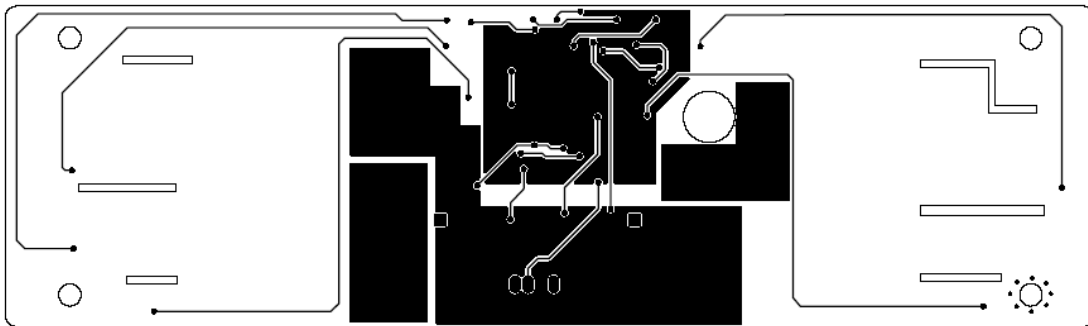
DVD board 2777C (Bottom layer view)



HI-voltage Board 2770C(Top layer view)



HI-voltage Board 2770C(Bottom layer view)



Part 2 Key ICs And Assemblies

On Main Board			On DVD board		
Serial No	Position	Type	Serial no	Position	Type
1	6U2	FSAV330	1	U1	BA033T
2	8U3	L7808C-V	2	U2	LM1117
3	2U1	AT49BV040B	3	U3	MT1389HD
4	2U3	FLI8125	4	U4	BA5954
5	1U6	FDS9435A	5	U5	BA6208F
6	1U1	AM1510	6	U6	K4S641632H
7	2U7	AT24C32A	7	U7	MX29LV160BT
8	1U2	AP1513S	8	U8	AT24C16
9	8U4	CD4052	9	U9	NJM4558
10	8U2	MSP3415G	10	U10	WM8714
11	9U1 9U2	TDA1517ATW			
12	4U2 6U1 6U3	PESD5VOL4U			
13	1U3	LM1117			
14	4U1	PESD5VOL5			
On HI-voltage Board			On VGA Board		
1	IC1	Bit3193	1	1U5	24C02
2	Q7,Q8	AP4511M	2	5D18	PESD5VOL4U

ICS ON MAIN BOARD

1. [FSAV330](#)

Low On Resistance Quad SPDT Wide Bandwidth Video Switch

General Description

The Fairchild Video Switch FSAV330 is a quad single pole/double throw high-speed CMOS TTL-compatible video switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

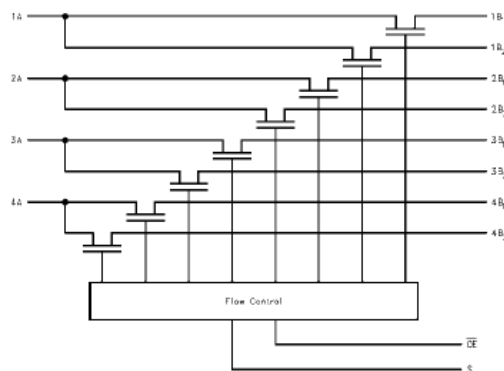
- Replacement for the P15V330
- Wide bandwidth 180 MHz
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level

Ordering Code:

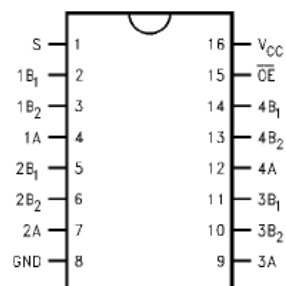
Order Number	Package Number	Package Description
FSAV330M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FSAV330QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSAV330MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B ₁ -B ₂	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	A = B ₁
H	L	A = B ₂

2. [FLI8125](#)

The FLI8125 is a cost-effective, highly-integrated, mixed signal solution for TV and Digital Video applications. It incorporates a multi-standard video decoder, high-speed triple 8-bit Analog-to-Digital Converter(ADC),and front end switching. An integrated VBI Slicer adds Closed Captioning(CC) and Teletext service support, and the built-in microprocessor enables full system control without external devices.

Features

INTEGRATED TRIPLE ADC ▪ RGB / YPbPr support up to 135MHz ▪ SCART – RGB + Fast Blank support ▪ Interlaced and progressive scan ▪ External OSD support DIGITAL INPUT PORT ▪ 24-bit re-configurable input port INTEGRATED 2D VIDEO DECODER ▪ Worldwide NTSC/PAL/SECAM support ▪ Macrovision / VCR trick mode support EMBEDDED MICROPROCESSOR ▪ Turbo 186 core ▪ Internal RAM / ROM ▪ Serial Flash / Parallel ROM support ▪ 2-wire slave controller, UART support ▪ Internal RESET Controller ▪ GPIOs , Low Bandwidth ADC – 6 input ▪ Infra-red Interface SCALING ENGINE ▪ Independent H & V scaling factors ▪ 4:2:2 YPbPr or 4:4:4 RGB scaling ▪ Anamorphic scaling (non-linear)	FAROUDJA DCDI – EDGE™ ▪ Edge Correction – Eliminates objectionable stair-casing – Enhances clarity and realism ▪ Horizontal Enhancement ▪ Adaptive Contrast and Color (ACC) ▪ Active Color Management - II (ACM-II) DIGITAL OUTPUT ▪ 18/24-bit 85Mhz TTL output ▪ Dual LVDS up to SXGA ▪ Energy Spectrum Management for reducing EMI ▪ Programmable CLUT for gamma correction OSD CONTROLLER ▪ Up to 4 windows: 1, 2 or 4-bits per pixel color ▪ Programmable Font scalar to meet Teletext requirements VBI SLICER ▪ V-Chip, Closed Captioning, XDS, CGMS, WSS decode ▪ Teletext 1.5 support JTAG SUPPORT ▪ Boundary Scan support
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- **Pinout**



- **Pin List**

I/O Legend: A = Analog, I = Input, O = Output, P = Power, G= Ground

Table 1: Analog Input Port

Pin Name	No.	I/O	Description
VDD18_A B	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
NC	159		No Connection. Leave this pin open for normal operation.
GND18_C	160	AG	Analog Ground (1.8V Return) for C channel. Must be directly connected to the analog system ground plane on board.
VDD18_C	161	AP	Analog Power (1.8V) for C Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
ADC_TES T	162	O	Analog Front End Test O/P. Leave this Pin open. Used for factory testing purpose only.
AVDD_AD C	163	AP	Analog Power (3.3V) for ADC. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AGND	164	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
AGND	165	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV1P	166	AI	Positive analog sync input for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.

GNDS	167	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A1P	168	AI	Positive analog input 'A' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	169	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B1P	170	AI	Positive analog input 'B' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	171	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C1P	172	AI	Positive analog input 'C' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_A	173	AP	Analog Power (3.3V) for ADC of Channel-A. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AN	174	AI	Negative analog input 'A' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-A Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	175	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV2P	176	AI	Positive analog sync input for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	177	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A2P	178	AI	Positive analog input 'A' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	179	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B2P	180	AI	Positive analog input 'B' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	181	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C2P	182	AI	Positive analog input 'C' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_B	183	AP	Analog Power (3.3V) for ADC of Channel-B. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
BN	184	AI	Negative analog input 'B' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-B Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	185	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV3P	186	AI	Positive analog sync input for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GNDS	187	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A3P	188	AI	Positive analog input 'A' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	189	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B3P	190	AI	Positive analog input 'B' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	191	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C3P	192	AI	Positive analog input 'C' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_C	193	AP	Analog Power (3.3V) for ADC of Channel-C. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
CN	194	AI	Negative analog input 'C' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-C Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	195	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV4P	196	AI	Positive analog sync input for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	197	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A4P	198	AI	Positive analog input 'A' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	199	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B4P	200	AI	Positive analog input 'B' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	201	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C4P	202	AI	Positive analog input 'C' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_SC	203	AP	Analog Power (3.3V) for ADC of SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.

SVN	204	AI	Negative analog sync input for channels 1 through 4. This acts as the return Path for the Sources connected to SV Channel Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
VO_GND	205	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
VOUT2	206	AO	Analog VOUT signal This is the Analog Video Output from the Decoder in the Composite Video format. This can be amplified and be fed to any video display device.
VDD18_SC	207	AP	Analog Power (1.8V) for SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GND18_SC	208	AG	Analog Ground (1.8V Return) for SYNC channel. Must be directly connected to the analog system ground plane on board.

Table 2: Low Bandwidth ADC Input Port

Pin Name	No	I/O	Description
VDDA33_LBADC	1	AP	Analog Power (3.3V) for Low Bandwidth ADC Block. Must be bypassed with 0.1uF capacitor.
LBADC_IN1	2	AI	Low Bandwidth Analog Input-1. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN2	3	AI	Low Bandwidth Analog Input-2. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN3	4	AI	Low Bandwidth Analog Input-3. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN4	5	AI	Low Bandwidth Analog Input-4. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN5	6	AI	Low Bandwidth Analog Input-5. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN6	7	AI	Low Bandwidth Analog Input-6. The Input signal connected to this Pin, must be bypassed with
LBADC_RTN	8	AG	This Pin provides the Return Path for LBADC inputs. Must be directly connected to the analog system ground plane on board.
VSSA33_LBADC	9	AG	Analog Ground for Low Bandwidth ADC Block. Must be directly connected to the analog system ground plane on board.

Table 3: RCLK PLL Pins

Pin Name	No	I/O	Description
GND_RPLL	11	DG	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD_RPLL_18	12	DP	Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to Ground Plane.
VBUFC_RPLL	13	O	Test Output. Leave this Pin Open. This is reserved for Factory Testing Purpose.
AGND_RPLL	14	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
XTAL	15	AO	Crystal oscillator output.
TCLK	16	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator.
AVDD_RPLL_33	17	AP	Analog Power (3.3V) for RCLK PLL. Must be bypassed with 0.1uF capacitor.

Table 4: Digital Video Input Port

Pin Name	No	I/O	Description
VID_CLK_1	153	I	Video port data clock input meant for Video Input – 1. Up to 75Mhz [Input, 5V-tolerant]
VIDIN_HS	122	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Horizontal Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Horizontal Sync Input for Video Input – 1. OR this Pin acts as Horizontal Sync Input for 24 Bit Video Input
VIDIN_VS	121	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Vertical Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Vertical Sync Input for Video Input – 1. OR this Pin acts as Vertical Sync Input for 24 Bit Video Input
VID_DATA_IN_0	135	IO	Input YUV data in 8-bit BT656 of Video Input – 1 [Bi-Directional, 5V-tolerant] OR Input Y Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Red Data in case of 24 Bit Video Input
VID_DATA_IN_1	136		
VID_DATA_IN_2	137		
VID_DATA_IN_3	138		
VID_DATA_IN_4	139		
VID_DATA_IN_5	140		
VID_DATA_IN_6	141		
VID_DATA_IN_7	142		

Pin Name	No	I/O	Description
VID_DATA_IN_8	145	IO	Input Pr / Pb Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Green Data in case of 24 Bit Video Input
VID_DATA_IN_9	146		
VID_DATA_IN_10	147		
VID_DATA_IN_11	148		
VID_DATA_IN_12	149		
VID_DATA_IN_13	150		
VID_DATA_IN_14	151		
VID_DATA_IN_15	152		
VID_DATA_IN_16	123	IO	Input Blue Data in case of 24 Bit Video Input OR Video Input – 2 in 8-bit with Embedded Sync / Separate Sync Sync in which case VID_DATA_IN_16 acts as the LSB of the 8-bit Video input and VID_DATA_IN_23 acts as the MSB of the 8-bit Video input.
VID_DATA_IN_17	124		
VID_DATA_IN_18	125		
VID_DATA_IN_19	128		
VID_DATA_IN_20	129		
VID_DATA_IN_21	130		
VID_DATA_IN_22	131		
VID_DATA_IN_23	132		
VID_CLK2	118	I	Video port data clock input meant for Video Input – 2. Up to 75Mhz [Input, 5V-tolerant]
VID_DE/FLD	115	I	Video Active Signal Input or the Field Signal Input from external Digital Video Source.

Note: In case of Multiple Digital Video Input Sources, only one source could be in 8-Bit with embedded Sync (BT656 mode) format.

Table 5: System Interface

Pin Name	No	I/O	Description
RESETn	10	I	Hardware Reset (active low) [Schmitt trigger, 5v-tolerant] Connect to ground with 0.01uF (or larger) capacitor.
TEST	20	I	For normal mode of operation connect this Pin to Ground.
GPIO15	21	IO	This pin is available as a general-purpose input/output port. Also it is optionally programmable to give out the external chip select signal meant for external SRAM. Refer to note below.
HSYNC2	22	I	Horizontal Sync signal Input-2. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC2	23	I	Vertical Sync signal Input-2. Used when Analog RGB component signal carries separate VSYNC signal.
HOST_SCLK	24	IO	Host input clock or 186 UART Data In or JTAG clock signal. [Input, Schmitt trigger, 5V-tolerant]
HOST_SDATA	25	IO	Host input data or 186 UART Data Out or JTAG mode signal. [Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant]
DDC_SCLK	26	IO	DDC2Bi clock for VGA Port [internal 10K Ω pull-up resistor]
DDC_SDATA	27	IO	DDC2Bi data for VGA Port [internal 10K Ω pull-up resistor]
MSTR_SCLK	30	O	Clock signal from Master Serial 2 Wire Interface Controller
MSTR_SDATA	31	IO	Data signal meant for Master Serial 2 Wire interface Controller
TCK	34	IO	This Pin accepts the Input Clock signal in case of Boundary Scan Mode.
TDI	35	IO	This Pin accepts the Input Data signal in case of Boundary Scan Mode.
TMS	36	IO	This Pin accepts the Input Test Mode Select signal in case of Boundary Scan Mode.
TRST	37	IO	This Pin accepts the Boundary Scan Reset signal in case of Boundary Scan Mode.
GPIO6/IRin	38	IO	Input from Infra Red Decoder can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO7/IRQin	41	IO	Input Interrupt Request signal can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO8/IRQout	42	IO	This Pin will give out the Interrupt Signal to interrupt external Micro. When not used, this pin is available as General Purpose Input/output Port.
GPIO9/SIPC_SCLK	43	IO	This Pin accepts the Clock signal from External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. When not used, this pin is available as General Purpose Input/output Port.
GPIO10/SIPC_SDATA/A18	44	IO	This Pin acts as the Data I/O signal when used with External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Or this Pin is programmable to give out Address # 18 from the Internal Micro when used with 512K External Memory. When not used, this pin is available as General Purpose Input/output Port.
GPIO11/PWM0	47	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO12/PWM1	48	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO13/PWM2	51	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.

Pin Name	No	I/O	Description
GPIO14/PWM3/SCART16	52	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Or it can be programmed to sense the Fast Blank Input signal from a SCART I/P source. When not used, this pin is available as General Purpose Input/output Port.
TDO	55	O	This Pin provides the Output Data in case of Boundary Scan Mode.
HSYNC1	156	I	Horizontal Sync signal Input-1. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC1	157	I	Vertical Sync signal Input-1. Used when Analog RGB component signal carries separate VSYNC signal.
101		O	Clock Output meant for External OSD Controller
102		O	Horizontal Sync Output meant for External OSD Controller
XOSD_CLK	103	O	Vertical Sync Output meant for External OSD Controller
XOSD_HS	104	O	Field Signal Output meant for External OSD Controller
PD20/B4/GPIO0 PD21/B5/GPIO1 PD22/B6/GPIO2 PD23/B7/GPIO3	86 87 88 89	IO	These Pins provide the Panel Data as shown in the TTL Display Interface Table below. These are available as General Purpose Input / Output Pins when not used as Panel Data.

Table 6: LVDS Display Interface

Pin Name	No	I/O	Description
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]
AVDD_LV_33	56	DP	Digital Power for LVDS Block. Connect to digital 3.3V supply.
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.
AVSS_LV	58	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	59	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_E	60	O	These form the Differential Data Output for Channel – 3 (Even).
CH3N_LV_E	61	O	
CLKP_LV_E	62	O	These form the Differential Clock Output Even Channel.
CLKN_LV_E	63	O	
CH2P_LV_E	64	O	These form the Differential Data Output for Channel – 2 (Even).
CH2N_LV_E	65	O	
CH1P_LV_E	66	O	These form the Differential Data Output for Channel – 1 (Even).
CH1N_LV_E	67	O	
CH0P_LV_E	68	O	These form the Differential Data Output for Channel – 0 (Even).
CH0N_LV_E	69	O	
AVSS_OUT_LV	70	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	71	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_O	72	O	These form the Differential Data Output for Channel – 3 (Odd).
CH3N_LV_O	73	O	
CLKP_LV_O	74	O	These form the Differential Clock Output Odd Channel.
CLKN_LV_O	75	O	
CH2P_LV_O	76	O	These form the Differential Data Output for Channel – 2 (Odd).
CH2N_LV_O	77	O	
CH1P_LV_O	78	O	These form the Differential Data Output for Channel – 1 (Odd).
CH1N_LV_O	79	O	
CH0P_LV_O	80	O	These form the Differential Data Output for Channel – 0 (Odd).
CH0N_LV_O	81	O	
AVSS_OUT_LV	82	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	83	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.

Table 7: TTL Display Interface

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]	
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]	
AVDD_LV_33	56	DP	Digital Power for TTL Block. Connect to digital 3.3V supply.	
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.	
AVSS_LV	58	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	59	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
R0	60	O	Red channel bit 0 (Even)	Not used.
R1	61	O	Red channel bit 1 (Even)	Not used.
R2	62	O	Red channel bit 2 (Even)	Red channel bit 0 (Even)
R3	63	O	Red channel bit 3 (Even)	Red channel bit 1 (Even)
R4	64	O	Red channel bit 4 (Even)	Red channel bit 2 (Even)
R5	65	O	Red channel bit 5 (Even)	Red channel bit 3 (Even)
R6	66	O	Red channel bit 6 (Even)	Red channel bit 4 (Even)
R7	67	O	Red channel bit 7 (Even)	Red channel bit 5 (Even)
G0	68	O	Green channel bit 0 (Even)	Not used.
G1	69	O	Green channel bit 1 (Even)	Not used.
AVSS_OUT_LV	70	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	71	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
G2	72	O	Green channel bit 2 (Even)	Green channel bit 0 (Even)
G3	73	O	Green channel bit 3 (Even)	Green channel bit 1 (Even)
G4	74	O	Green channel bit 4 (Even)	Green channel bit 2 (Even)
G5	75	O	Green channel bit 5 (Even)	Green channel bit 3 (Even)
G6	76	O	Green channel bit 6 (Even)	Green channel bit 4 (Even)
G7	77	O	Green channel bit 7 (Even)	Green channel bit 5 (Even)
B0	78	O	Blue channel bit 0 (Even)	Not used.
B1	79	O	Blue channel bit 1 (Even)	Not used.
B2	80	O	Blue channel bit 2 (Even)	Blue channel bit 0 (Even)
B3	81	O	Blue channel bit 3 (Even)	Blue channel bit 1 (Even)
AVSS_OUT_LV	82	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	83	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
PD20/B4	86	O	Blue channel bit 4 (Even)	Blue channel bit 2 (Even)
PD21/B5	87	O	Blue channel bit 5 (Even)	Blue channel bit 3 (Even)
PD22/B6	88	O	Blue channel bit 6 (Even)	Blue channel bit 4 (Even)
PD23/B7	89	O	Blue channel bit 7 (Even)	Blue channel bit 5 (Even)
DEN	90	O	Display Data Enable	
DHS	91	O	Display Horizontal Sync.	
DVS	92	O	Display Vertical Sync.	
DCLK	93	O	Display Pixel Clock	
PD24	115	O	Red channel bit 0 (Odd)	Not used.
Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PD25	114	O	Red channel bit 1 (Odd)	Not used.
PD26	113	O	Red channel bit 2 (Odd)	Red channel bit 0 (Odd)
PD27	112	O	Red channel bit 3 (Odd)	Red channel bit 1 (Odd)
PD28	111	O	Red channel bit 4 (Odd)	Red channel bit 2 (Odd)
PD29	110	O	Red channel bit 5 (Odd)	Red channel bit 3 (Odd)
PD30	109	O	Red channel bit 6 (Odd)	Red channel bit 4 (Odd)
PD31	108	O	Red channel bit 7 (Odd)	Red channel bit 5 (Odd)
PD32	107	O	Green channel bit 0 (Odd)	Not used.
PD33	106	O	Green channel bit 1 (Odd)	Not used.
PD34	105	O	Green channel bit 2 (Odd)	Green channel bit 0 (Odd)
PD35	104	O	Green channel bit 3 (Odd)	Green channel bit 1 (Odd)
PD36	103	O	Green channel bit 4 (Odd)	Green channel bit 2 (Odd)
PD37	102	O	Green channel bit 5 (Odd)	Green channel bit 3 (Odd)
PD38	101	O	Green channel bit 6 (Odd)	Green channel bit 4 (Odd)
PD39	123	O	Green channel bit 7 (Odd)	Green channel bit 5 (Odd)
PD40	124	O	Blue channel bit 0 (Odd)	Not used.
PD41	125	O	Blue channel bit 1 (Odd)	Not used.
PD42	128	O	Blue channel bit 2 (Odd)	Blue channel bit 0 (Odd)
PD43	129	O	Blue channel bit 3 (Odd)	Blue channel bit 1 (Odd)
PD44	130	O	Blue channel bit 4 (Odd)	Blue channel bit 2 (Odd)
PD45	131	O	Blue channel bit 5 (Odd)	Blue channel bit 3 (Odd)

PD46	132	O	Blue channel bit 6 (Odd)	Blue channel bit 4 (Odd)
PD47	118	O	Blue channel bit 7 (Odd)	Blue channel bit 5 (Odd)

Note: In case of 24 Bit TTL Panels the RGB Odd Channel Outputs will not be used. In that case they can be made available for other purposes as Address & Data from On-Chip Micro or Digital Video Input Data.

Table 8: Parallel/Serial ROM Interface

Pin Name	No	I/O	Description
A17	95	O	256K x8 PROM Address. These pins also have bootstrap functionality. For serial SPI ROM interface: - ROM_ADDR17 will be Serial Clock (ROM_SCLK) - ROM_ADDR16 will be Serial Data Output (ROM_SDO) For 512K X 8 PROM, Address Signal A18 is available thru Pin # 44 which is GPIO10.
A16	96		
A15	100		
A14	101		
A13	102		
A12	103		
A11	104		
A10	105		
A9	106		
A8	107		
A7	108		
A6	109		
A5	110		
A4	111		
A3	112		
A2	113		
A1	114		
A0	115		
D7	132	IO	External PROM data input.
D6	131		
D5	130		
D4	129		
D3	128		
D2	125		
D1	124		
D0	123		
ROM_OEN	118	O	External PROM data Output Enable.
ROM_SDI/ ROM_WEN	97	O	External PROM data Write Enable (for In-System-Programming of FLASH) or Serial Data Input (SDI) for SPI ROM interface.
ROM_SCSN/ ROM_CSN	94	O	External PROM data Chip Select or Serial PROM Chip Select (ROM_SCSN) for SPI ROM interface.

Table 9: Digital Power and Ground

Pin Name	No	I/O	Description
RVDD_3.3	32 49 98 116 154	P	Ring VDD. Connect to digital 3.3V.
CVDD_1.8	18 28 39 45 84 119 126 133 143	P	Core VDD. Connect to digital 1.8V.
CRVSS	19 29 33 40 46 50 85 99 117 120 127 134 144 155	G	Chip ground for core and ring.

Table 10: JTAG Boundary Scan

Pin Name	No	I/O	Description
TCK	34	I	JTAG Boundary Scan TCK signal
TDO	55	O	JTAG Boundary Scan TDO signal
TDI	35	I	JTAG Boundary Scan TDI signal. Pad has internal 50K pull-up resistor.
TMS	36	I	JTAG Boundary Scan RST signal. Pad has internal 50K pull-up resistor.
TRST	37	I	JTAG Boundary Scan TMS signal. Pad has internal 50K pull-up resistor.

3. [FDS9435A](#) Single P-Channel Enhancement Mode Field Effect Transistor

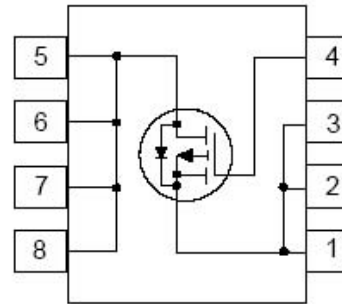
SO-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

• Features

-5.3 A, -30 V, $R_{DS(ON)} = 0.045 \Omega @ V_{GS} = -10 \text{ V}$,
 $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -4.5 \text{ V}$.

High density cell design for extremely low $R_{DS(ON)}$.

High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted			
Symbol	Parameter	FDS9435A	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	-20	V
I_D	Drain Current - Continuous (Note 1a)	-5.3	A
	- Pulsed	-50	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

4. [AT24C32A](#) 2-Wire Serial EEPROM 32K (4096 x 8)

Features

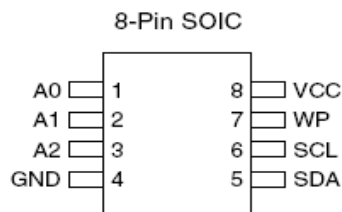
- **Low-Voltage and Standard-Voltage Operation**
 - 2.7 ($V_{CC} = 2.7V$ to $5.5V$)
 - 1.8 ($V_{CC} = 1.8V$ to $5.5V$)
- **Low-Power Devices ($I_{SB} = 2 \mu A$ @ $5.5V$) Available**
- **Internally Organized 4096 x 8, 8192 x 8**
- **2-Wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V) and 400 kHz (2.5V) Clock Rate for AT24C32A**
- **400 kHz (1.8V) Clock Rate for AT24C64A**
- **Write Protect Pin for Hardware Data Protection**
- **32-Byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
 - **Endurance: 1 Million Write Cycles**
 - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin JEDEC PDIP and 8-Pin JEDEC SOIC Packages**

Description

The AT24C32A/64A provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32A/64A is available in space saving 8-pin JEDEC PDIP and 8-pin JEDEC SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A₂, A₁, and A₀ are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited. If left unconnected, WP is internally pulled down to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

No.	Parameter	Symbol	SW		Input Conditions	Measurement
			1	2		
1	Total circuit	I _{CC}	-	-	V _i (SIF)=90dB μ V f=4.5MHz	Pin 19 current
2	Monaural output level	V _{0(Mon)}	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	AC voltmeter reading
3	Monaural frequency response 1	V _{1(Mon)}	b/c	a	(Monaural) 300Hz/1kHz, 30%mod 15kHz	Voltage ratio of 300Hz level to 1kHz level
4	Monaural frequency response 2	V _{2(Mon)}	b/c	a	(Monaural) 10Hz/1kHz, 30%mod 15kHz	Voltage ratio of 10kHz level to 1kHz level
5	Monaural Total Harmonic Distortion	THD _(Mon)	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	Distortion meter reading
6	Monaural S/N Ratio	V _{n(Mon)}	b/c	b	S: Monaural, 1kHz, 30%mod N: no signal CCIR filter, Q-PEAK response	AC voltmeter reading
7	L/R Channel Balance	V _{LR(Mon)}	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	Voltage ratio of left-channel signal to right-channel signal
8	Stereo output level	V _{0(st)}	b/c	a	(L(R)-only) 1kHz, 100%mod 15kHz LPF	AC voltmeter reading
9	Stereo frequency response 1	V _{1(st)}	b/c	a	(L(R)-only) 300Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 300Hz level to 1kHz level
10	Stereo frequency response 2	V _{2(st)}	b/c	a	(L(R)-only) 10Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 10kHz level to 1kHz level
11	Stereo Total Harmonic Distortion	THD _(st)	b/c	a	(L(R)-only) 1kHz, 100%mod 15kHz LPF	Distortion meter reading
12	Stereo S/N Ratio	V _{n(st)}	b/c	b	S: L(R)-only, 1kHz, 30%mod N: Pilot signal CCIR filter, Q-PEAK response	AC voltmeter reading
13	Stereo Sensitivity	V _{TH(st)}	-	-	Pilot signal	Input level at stereo read resistor comes to more than 3V.
14	Stereo hysteresis	V _{HY(st)}	-	-	Pilot signal	Input level at stereo read resistor comes to less than 1.5V.
15	Stereo Separation 1	SEP1	b/c	a	(L(R)-only) 400Hz, 30%mod 15kHz LPF	Voltage ratio of left-channel signal to right-channel signal
16	Stereo Separation 2	SEP2	b/c	a	(L(R)-only) 2kHz, 30%mod 15kHz LPF	Voltage ratio of left-channel signal to right-channel signal
17	SAP output level	V _{0(SAP)}	b/c	a	(SAP) 1kHz, 100%mod 15kHz LPF	AC voltmeter reading
18	SAP frequency response 1	V _{1(SAP)}	b/c	a	(SAP) 300Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 300Hz level to 1kHz level
19	SAP frequency response 2	V _{2(SAP)}	b/c	a	(SAP) 8kHz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 8kHz level to 1kHz level
20	SAP Total Harmonic Distortion	THD _(SAP)	b/c	a	(SAP) 1kHz, 100%mod 15kHz LPF	Distortion meter reading

5. [LM1117](#) (SOT-223)

FEATURES

- Output Current up to 1 A
- Low Dropout Voltage (700mV at 1A Output Current)
- Three Terminal Adjustable or Fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- 2.85V Device for SCSI-II Active Terminator
- 0.04% Line Regulation, 0.1% Load Regulation
- Very Low Quiescent Current
- Internal Current and Terminal Limit
- Logic-Controlled Electronics Shutdown
- Surface Mount Package SOT-223 & TO-263 (D2-Pack)
- 100% Thermal Limit Burn-In

APPLICATION

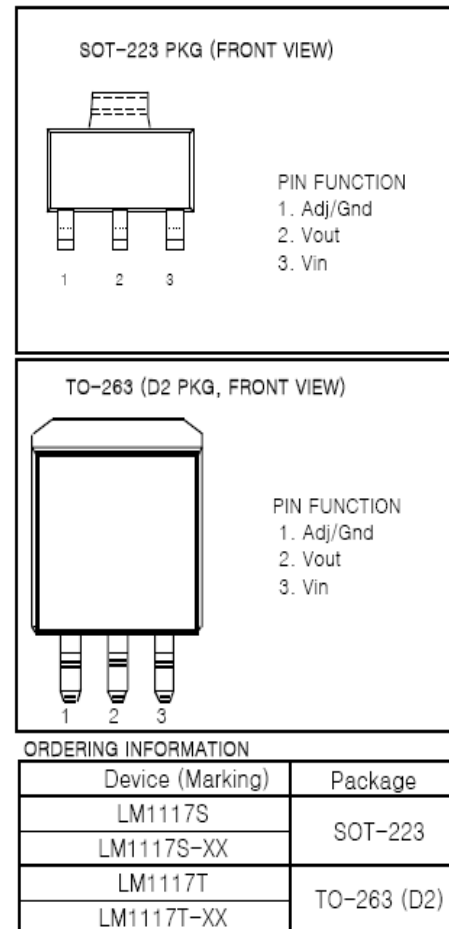
- Active SCSI Terminators
- Portable/Plan Top/Notebook Computers
- High Efficiency Linear Regulators
- SMPS Post Regulators
- Mother B/D Clock Supplies
- Disk Drives
- Battery Chargers

DESCRIPTION

The LM1117 is a low power positive-voltage regulator designed to meet 1A output current and comply with SCSI-II specifications with a fixed output voltage of 2.85V. This device is an excellent choice for use in battery-powered applications, as active terminators for the SCSI bus, and portable computers.

The LM1117 features very low quiescent current and very low **dropout voltage of 700mV at a full load** and lower as output current decreases. LM1117 is available as an adjustable or fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 5.0V output voltages.

The LM1117 is offered in a 3-pin surface mount package SOT-223 & TO-263. The output capacitor of 10 μ F or larger is needed for output stability of LM1117 as required by most of the other regulator circuits.



(X=Output Voltage=1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V, Adjustable=AD)

ICS ON DVD BOARD

1. [BA033T](#) Low saturation voltage type 3-pin regulator

The BA00T and BA00FP series are fixed positive output low drop-out type, 3-pin voltage regulators with positive output. These regulators are used to provide a stabilized output voltage from a fluctuating DC input voltage. There are 10 fixed output voltages, as follows: 3V, 3.3V, 5V, 6V*, 7V, 8V, 9V, 10V, 12V and 15V. The maximum current capacity is 1A for each of the above voltages. (Items marked with an asterisk are under development.)

●Application

Constant voltage power supply

●Features

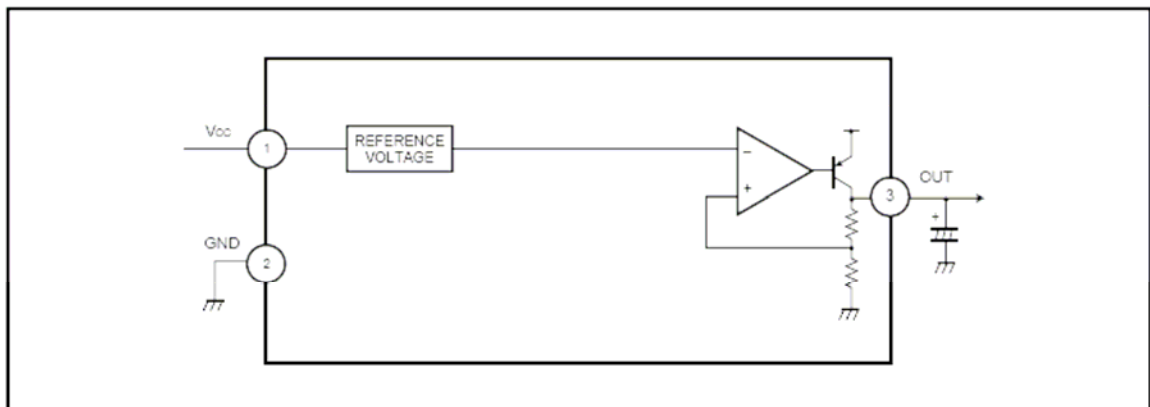
- 1) Built-in overvoltage protection circuit, overcurrent protection circuit and thermal shutdown circuit.
- 2) TO220FP and TO252-3 packages are available to cover a wide range of applications.
- 3) Compatible with the BA17800 series.
- 4) Richly diverse lineup.
- 5) Low minimum I / O voltage differential.

●Product codes

Output voltage (V)	Product No.	Output voltage (V)	Product No.
3.0	BA03T / FP	8.0	BA08T / FP
3.3	BA033T / FP	9.0	BA09T / FP
5.0	BA05T / FP	10.0	BA10T / FP
6.0	BA06T * / FP *	12.0	BA12T / FP
7.0	BA07T / FP	15.0	BA15T / FP

* : Under development.

●Block diagram



2. [LM1117](#) (See Page 21)

3. [MT1389HD](#)

Abbr. :

SR : Slew Rate

PU : Pull Up

PD : Pull Down

SMT : Schmitt Trigger

2MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (26)				
231	RFGND18		Ground	Analog ground
232	RFVDD18		Power	Analog power 1.8V
252	OSP		Analog output	RF Offset cancellation capacitor connecting
253	OSN		Analog output	RF Offset cancellation capacitor connecting
254	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input

ALPC (4)				
Pin	Main	Alt.	Type	Description
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output

23	LDO1		Analog Output	Laser driver output
ADC Power (2)				
244	ADCVDD3		Power	Analog 3.3V Power for ADC
245	ADCVSS		Ground	Analog ground for ADC
VPLL (3)				
43	VPLLVSS		Ground	Analog ground for VPLL
44	CAPPAD		Analog Inout	VPLL External Capacitance connection
45	VPLLVDD3		Power	Analog 3.3V Power for VPLL
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) 2) Central servo Positive main beam summing output
26	RFLVL	RFON	Analog output	1) 2) RFRP low pass, or Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (6)				
246	RFVDD3		Power	Analog Power
247	RFRPDC		Analog output	RF ripple detect output
248	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
249	HRFZC		Analog Input	High frequency RF ripple zero crossing
250	CRTPLP		Analog output	Defect level filter capacitor connecting
251	RFGND		Ground	Analog Power

RF Data PLL Interface (9)				
Pin	Main	Alt.	Type	Description
235	JITFO		Analog output	The output terminal of RF jitter meter.
236	JITFN		Analog Input	The input terminal of RF jitter meter.
237	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.
238	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
239	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
240	LPFON		Analog Output	The negative output of loop filter amplifier
241	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
242	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
243	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENP W M		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT 1	V_ADIN9	Analog Output	1) 1st General PWM output, or 2) Version AD input 9
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
50	FG (Diogital pin)	V_ADIN8	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for V_ADIN8	1) Motor Hall sensor input, or 2) Version AD input 8
General Power/Ground (18)				
55,93, 142,160, 174, 213	DVDD18		Power	1.8V power pin for internal digital circuitry
81,178	DVSS		Ground	1.8V Ground pin for internal digital circuitry
65,96,11 8, 131,145, 156, 170, 208	DVDD3		Power	3.3V power pin for internal digital circuitry
90, 148	DVSS		Ground	3.3V Ground pin for internal digital circuitry

Micro Controller and Flash Interface (48)				
Pin	Main	Alt.	Type	Description
62	HIGHA0		Inout 2~16MA, SR PU	Microcontroller address 8
74	HIGHA1		Inout 2~16MA, SR PU	Microcontroller address 9
73	HIGHA2		Inout 2~16MA, SR PU	Microcontroller address 10
72	HIGHA3		Inout 2~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Inout 2~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Inout 2~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Inout 2~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Inout 2~16MA, SR PU	Microcontroller address 15
89	AD7		Inout 2~16MA, SR	Microcontroller address/data 7
86	AD6		Inout 2~16MA, SR	Microcontroller address/data 6
85	AD5		Inout 2~16MA, SR	Microcontroller address/data 5
84	AD4		Inout 2~16MA, SR	Microcontroller address/data 4
83	AD3		Inout 2~16MA, SR	Microcontroller address/data 3
82	AD2		Inout 2~16MA, SR	Microcontroller address/data 2
80	AD1		Inout 2~16MA, SR	Microcontroller address/data 1
79	AD0		Inout 2~16MA, SR	Microcontroller address/data 0

92	IOA0		Inout 2~16MA, SR PU	Microcontroller address 0 / IO
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Pin	Main	Alt.	Type	Description
77	IOA1		Inout 2~16MA, SR PU	Microcontroller address 1 / IO
56	IOA2		Inout 2~16MA, SR PU	Microcontroller address 2 / IO
57	IOA3		Inout 2~16MA, SR PU	Microcontroller address 3 / IO
58	IOA4		Inout 2~16MA, SR PU	Microcontroller address 4 / IO
59	IOA5		Inout 2~16MA, SR PU	Microcontroller address 5 / IO
60	IOA6		Inout 2~16MA, SR PU	Microcontroller address 6 / IO
61	IOA7		Inout 2~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Output 2~16MA, SR	Flash address 16
91	A17		Output 2~16MA, SR	Flash address 17
63	IOA18		Inout 2~16MA, SR SMT	Flash address 18 / IO
64	IOA19		Inout 2~16MA, SR SMT	Flash address 19 / IO
75	IOA20		Inout 2~16MA, SR SMT	Flash address 20 / IO

87	IOA21		Inout 2~16MA, SR SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: I) GPIO
88	ALE		Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable

Pin	Main	Alt.	Type	Description
78	IOOE#		Inout 2~16MA, SR SMT	Flash output enable, active low / IO
66	IOWR#		Inout 2~16MA, SR SMT	Flash write enable, active low / IO
76	IOCS#		Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO
94	UWR#		Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
95	URD#		Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
97	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
98	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
99	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
100	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
101	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I ² C clock pin
102	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I ² C data pin

103	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
104	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
105	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I ² C clock pin
106	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I ² C data pin
109	IR		Input SMT	IR control signal input
110	INTO#		Inout 4MA, SR PU, SMT	Microcontroller external interrupt 0, active low

Audio interface (28)				
Pin	Main	Alt.	Type	Description
204	SPMCLK	SCLK0	Inout Non-pull	1) Audio DAC master clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 clock pin II) GPIO
205	SPDATA	SDIN0	Inout Non-pull	1) Audio data of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-in II) GPIO
206	SPLRCK	SDO0	Inout Non-pull	1) Audio left/right channel clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-out II) GPIO
207	SPBCK	SDCS0 ASDATA5	Inout Non-pull	1) Audio bit clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 chip select II) Audio serial data 5 part I : DSD data sub-woofer channel or Microphone output III) GPIO

209	ALRCK		Inout 4MA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I) 1 : use external 373 II) 0: use internal 373
210	ABCK	Fs64	Output 4MA Non-pull	1) Audio bit clock 2) Phase de-modulation
211	ACLK		Inout 4MA Non-pull	Audio DAC master clock
197	ASDATA0		Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) DSD data left channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While using external channels: I) GPO_2
202	ASDATA1		Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) DSD data right channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While using external channels: I) GPO_1
203	ASDATA2		Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) DSD data left surround channel 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While using external channels: I) GPO_0 4)
212	ASDATA3		Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) DSD data right surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPO_0
214	ASDATA4	INT1#	Inout 4MA PD SMT	1) Audio serial data 4 (Down-mixed Left/Right) 2) DSD data center channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) Microcontroller external interrupt 1 II) GPO_0
215	MC_DATA	INT2#	Inout PD SMT	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPO_0

216	SPDIF		Output 2~16MA, SR : ON/OFF Non-pull	SPDIF output
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217	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
218	APLLCAP		Analog Inout	APLL External Capacitance connection
219	APLLVSS		Ground	Ground pin for audio clock circuitry
220	ADACVSS2		Ground	Ground pin for AUDIO DAC circuitry
221	ADACVSS1		Ground	Ground pin for AUDIO DAC circuitry
222	ARF	GPIO	Output	1) AUDIO DAC Sub-woofer channel output While internal 2) AUDIO DAC not used: GPIO
223	ARS	GPIO	Output	1) AUDIO DAC Right Surround channel output 2) While internal AUDIO DAC not used: a. SDATA3 b. GPIO
224	AR	GPIO	Output	1) AUDIO DAC Right channel output 2) While internal AUDIO DAC not used: a. SDATA1 b. GPIO
225	AVCM		Analog	AUDIO DAC reference voltage
226	AL	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA2 b. GPIO
227	ALS	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA0 b. GPIO
228	ALF	GPIO	Output	1) AUDIO DAC Center channel output 2) While internal AUDIO DAC not used:GPIO
229	ADACVDD1		Power	3.3V power pin for AUDIO DAC circuitry
230	ADACVDD2		Power	3.3V power pin for AUDIO DAC circuitry

Video Interface (18)				
196	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
195	VREF		Analog	Bandgap reference voltage
194	FS		Analog	Full scale adjustment
193	YUV0	CIN	Output 4MA, SR	1) Video data output bit 0 2) Compensation capacitor
192	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
191	YUV1	Y	Output 4MA, SR	1) Video data output bit 1 2) Analog Y output
190	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
189	YUV2	C	Output 4MA, SR	1) Video data output bit 2 2) Analog chroma output
188	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry

187	YUV3	CVBS	Output 4MA, SR	1) Video data output bit 3 2) Analog composite output
186	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
185	YUV4	Y/G	Output 4MA, SR	1) Video data output bit 4 2) Green or Y
184	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
183	YUV5	B/Cb/Pb	Output 4MA, SR	1) Video data output bit 5 2) Blue or CB
182	YUV6	R/Cr/Pr	Output 4MA, SR	1) Video data output bit 6 2) Red or CR
181	VSYN	V_ADIN1	Inout 4MA, SR SMT Non-pull	1) Vertical sync input/output 2) While no External TV-encoder: I) Vertical sync for video-input II) Version AD input port 1 III) GPIO
180	YUV7	INT3# ASDATA5	Inout 4MA, SR SMT Non-pull	1) Video data output bit 7 2) While no External TV-encoder: I) Microcontroller external interrupt 3 II) Audio serial data 5 part II : DSD data sub-woofer channel or Microphone output III) GPIO
179	HSYN	INT4# V_ADIN2	Inout 4MA, SR SMT Non-pull	1) Horizontal sync input/output 2) While no External TV-encoder: I) Horizontal sync for video-input II) Microcontroller external interrupt 4 III) Version AD input port 2 IV) GPIO
MISC (12)				
46	USB_VSS		USB Ground	USB ground pin
47	USBP		Analog Inout	USB port DPLUS analog pin
48	USBM		Analog Inout	USB port DMINUS analog pin
49	USB_VDD3		USB Power	USB Power pin 3.3V
108	PRST#		Input PU, SMT	Power on reset input, active low
107	ICE		Input PD, SMT	Microcontroller ICE mode enable
233	XTALO		Output	27M crystal out
234	XTALI		Input	27M crystal in
201	GPIO_3		Inout Pull-Down	GPIO
200	GPIO_4		Inout Pull-Down	GPIO
199	RCLKB	GPIO_5	Inout Pull-Up	GPIO
198	RVREF	GPIO_6	Inout Pull-Up	GPIO

Dram Interface (58) (Sorted by position)				
176	C_0	IO_0 (RD16)	Inout Non-pull	1) Digital Video output C bit 0 2) GPIO
175	C_1	IO_1 (RD17)	Inout Non-pull	1) Digital Video output C bit 1 2) GPIO
173	C_2	IO_2 (RD18)	Inout Non-pull	1) Digital Video output C bit 2 2) GPIO
172	C_3	IO_3 (RD19)	Inout Non-pull	1) Digital Video output C bit 3 2) GPIO
171	C_4	IO_4 (RD20)	Inout Non-pull	1) Digital Video output C bit 4 2) GPIO
169	C_5	IO_5 (RD21)	Inout Non-pull	1) Digital Video output C bit 5 2) GPIO
168	C_6	IO_6 (RD22)	Inout Non-pull	1) Digital Video output C bit 6 2) GPIO
167	C_7	IO_7 (RD23)	Inout Non-pull	1) Digital Video output C bit 7 2) GPIO

177	IO_17	(DQM2)	Inout Non-pull	GPIO
166	YUVCLK	IO_8 (DQM3)	Inout Non-pull	1) Digital Video output Clock 2) GPIO
165	Y_0	IO_9 (RD24)	Inout Non-pull	1) Digital Video output Y bit 0 2) GPIO
164	Y_1	IO_10 (RD25)	Inout Non-pull	1) Digital Video output Y bit 1 2) GPIO
163	Y_2	IO_11 (RD26)	Inout Non-pull	1) Digital Video output Y bit 2 2) GPIO
162	Y_3	IO_12 (RD27)	Inout Non-pull	1) Digital Video output Y bit 3 2) GPIO
161	Y_4	IO_13 (RD28)	Inout Non-pull	1) Digital Video output Y bit 4 2) GPIO
159	Y_5	IO_14 (RD29)	Inout Non-pull	1) Digital Video output Y bit 5 2) GPIO
158	Y_6	IO_15 (RD30)	Inout Non-pull	1) Digital Video output Y bit 6 2) GPIO
157	Y_7	IO_16 (RD31)	Inout Non-pull	1) Digital Video output Y bit 7 2) GPIO

155	RA4		Inout	DRAM address 4
154	RA5		Inout	DRAM address 5
153	RA6		Inout	DRAM address 6
152	RA7		Inout	DRAM address 7

151	RA8		Inout	DRAM address 8
150	RA9		Inout	DRAM address 9
149	RA11		Inout Pull-Down	DRAM address bit 11

147	CKE		output	DRAM clock enable
146	RCLK		Inout	Dram clock
144	RA3		Inout	DRAM address 3
143	RA2		Inout	DRAM address 2
141	RA1		Inout	DRAM address 1
140	RA0		Inout	DRAM address 0
139	RA10		Inout	DRAM address 10
138	BA1		Inout	DRAM bank address 1
137	BA0		Inout	DRAM bank address 0
136	RCS#		output	DRAM chip select, active low
135	RAS#		output	DRAM row address strobe, active low
134	CAS#		output	DRAM column address strobe, active low
133	RWE#		output	DRAM Write enable, active low
132	DQM1		Inout	Data mask 1
130	IO_18	(DQS1)	Inout Non-pull	GPIO
129	RD8		Inout	DRAM data 8
128	RD9		Inout	DRAM data 9

127	RD10		Inout	DRAM data 10
126	RD11		Inout	DRAM data 11
125	RD12		Inout	DRAM data 12
124	RD13		Inout	DRAM data 13
123	RD14		Inout	DRAM data 14
122	RD15		Inout	DRAM data 15
121	RD0		Inout	DRAM data 0
120	RD1		Inout	DRAM data 1
119	RD2		Inout	DRAM data 2
117	RD3		Inout	DRAM data 3
116	RD4		Inout	DRAM data 4
115	RD5		Inout	DRAM data 5
114	RD6		Inout	DRAM data 6
113	RD7		Inout	DRAM data 7
112	IO_19	(DQS0)	Inout Non-pull	GPIO
111	DQM0		Inout	Data mask 0

JTAG Interface(4)					
51	TDI	V_ADIN4	Inout Non-pull	1) 2) 3)	Serial interface port 3 data-out Version AD input port 4 GPIO
52	TMS	V_ADIN5	Inout Non-pull	1) 2) 3)	Serial interface port 3 data-in Version AD input port 5 GPIO
53	TCK	V_ADIN6	Inout Non-pull	1) 2) 3)	Serial interface port 3 clock pin Version AD input port 6 GPIO
54	TDO	V_ADIN7	Inout Non-pull	1) 2) 3)	Serial interface port 3 chip-select Version AD input port 7 GPO

Note:

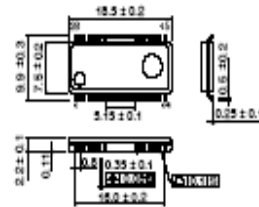
1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to **green characters**.
3. The video input port and external TV encoder mode can not both use CCIR-601 mode, at least one of them should be in CCIR-656 mode.
4. Following is a summary of modified pins.
 - (a) Pin 48, 49, 50, 51 are no longer for JTAG functions.
 - (b) V_ADIN0 and V_ADIN3 is not available.

4. [BA5954](#)

● Description

BA5954FP/FM is an actuator driver IC for CD-ROM and DVD players. This actuator driver adopts current feedback system. This IC incorporates 2 channel actuator drivers and 2 channel motor drivers. Current phase lag influenced load inductance is little, because this type is current feedback.

● Dimension (Units : mm)



HSOP28 / HSOP-M28

● Features

- 1) Wide dynamic range
 $V_{OM}4.0V(\text{typ.})$ at $PreV_{CC}=12V, PV_{CC}=5V, R_L=8\Omega$
- 2) Level shift circuit built in.
- 3) Thermal-shut-down circuit built in.
- 4) Stand-by mode built in.

● Applications

CD/CD-ROM

● Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Supply voltage	$V_{CC}, PV_{CC1/2}$	18	V
Power dissipation	P_d	(BA5954FP) *1 1.7	W
		(BA5954FM) *2 2.2	
Operating temperature range	T_{opr}	$-35 \sim +85$	$^\circ\text{C}$
Storage temperature range	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

* PCB (70mmx70mm, $z=1.6\text{mm}$) glass epoxy mounting.

*1 Derating : 18.6mW/ $^\circ\text{C}$ for operation above $T_a=25^\circ\text{C}$

*2 Derating : 17.6mW/ $^\circ\text{C}$ for operation above $T_a=25^\circ\text{C}$

● Recommended Operating Conditions ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	4.3 ~ 13.2	V
	PV_{CC1}	4.3 ~ V_{CC}	V
	PV_{CC2}	4.3 ~ V_{CC}	V

5. BA6208F

The BA6208F is monolithic ICs used for driving reversible motors. It allows control of reversible motors in cassette players and other electrical equipment by using TTL-level logic signals. The IC contains a logic section, which controls forward and reverse rotations as well as forced stop, and an output power section, which can supply an output current of up to 100mA (typical) according to the logic control.

●Features

- 1) Motor driving power transistors are built in (100mA typically).
- 2) Brake is applied when stopping the motor (when inputs A and B are both HIGH level).
- 3) Built-in diode to absorb surge currents.
- 4) Very low standby circuit current when inputs A and B are both LOW level.
- 5) Wide range of operating supply voltage (4.5 ~ 15.0V).
- 6) Direct control with the TTL logic.

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V _{CC}	18	V
Power dissipation	BA6208	P _d	700*1	mW
	BA6208F	P _d	450*2	
Operating temperature		T _{opr}	-20~+60	°C
Storage temperature		T _{stg}	-55~+125	°C
Maximum output current		I _{OUT}	500	mA

* 1 Reduced by 7 mW for each increase in Ta of 1°C over 25°C.

* 2 Reduced by 4.5 mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	4.5	—	15	V

●Input truth table

3pin (Ain)	2pin (Bin)	8pin (Aout)	7pin (Bout)
H	L	H	L
L	H	L	H
H	H	L	L
L	L	OPEN	OPEN

Note : HIGH level input is 2.0 V or more.

LOW level input is 0.8 V or less.

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{CC} = 9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output current	I _O	200	—	—	mA	
Output saturation voltage	V _{CE}	—	—	1.6	V	I _O =100mA
Input high level voltage	V _{IH}	2.0	—	—	V	
Input low level voltage	V _{IL}	—	—	0.8	V	
Standby supply current	I _{ST}	—	—	0.4	mA	When inputs A and B are both LOW level
Input high level current	I _{IH}	—	—	400	μA	V _{IH} =4.5V

A diode that absorbs at least 500 mA is built in to give protection against surge currents with a pulse width of 10 ms and a duty ratio of 10% or less.

6. [K4S641632H-TC60](#) SDRAM 64Mb H-die(x16)

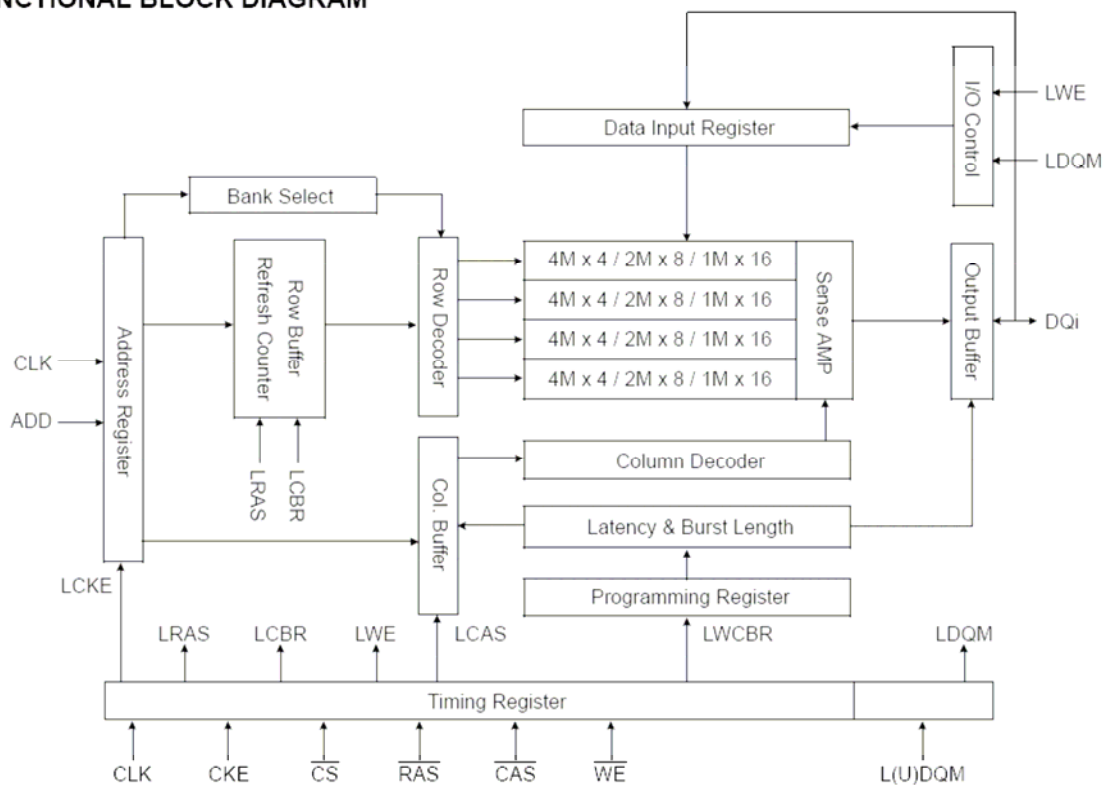
The K4S641632H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

• Information

Part No.	Organization	Max Freq	Interface	Package
K4S641632H-TC(L)60	4Mb x 16	166MHz(CL=3)	LVTTTL	54 pin TSOP(II)
K4S641632H-TC(L)60	4Mb x 16	166MHz(CL=3)	LVTTTL	54 pin TSOP(II)

Row Address	Column Address
A0~A11	A0~A9

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

• Pin Configuration (top view)

VDD	1	54	VSS
DQ0	2	53	DQ15
VDDQ	3	52	VSSQ
DQ1	4	51	DQ14
DQ2	5	50	DQ13
VSSQ	6	49	VDDQ
DQ3	7	48	DQ12
DQ4	8	47	DQ11
VDDQ	9	46	VSSQ
DQ5	10	45	DQ10
DQ6	11	44	DQ9
VSSQ	12	43	VDDQ
DQ7	13	42	DQ8
VDD	14	41	VSS
LDQM	15	40	N.C/RFU
WE	16	39	UDQM
CAS	17	38	CLK
RAS	18	37	CKE
CS	19	36	N.C
BA0	20	35	A11
BA1	21	34	A9
A10/AP	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
VDD	27	28	VSS

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A ₀ ~ A ₁₁	Address	Row/column addresses are multiplexed on the same pins. Row address : RA ₀ ~ RA ₁₁ , Column address : (x4 : CA ₀ ~ CA ₃ , x8 : CA ₀ ~ CA ₃ , x16 : CA ₀ ~ CA ₇)
BA ₀ ~ BA ₁	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	Data input/output mask	Makes data output Hi-Z, t _{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ ₀ ~ N	Data input/output	Data inputs/outputs are multiplexed on the same pins. (x4 : DQ ₀ ~ 3), (x8 : DQ ₀ ~ 7), (x16 : DQ ₀ ~ 15)
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

7. [MX29LV160BT](#)

16M-BIT[2Mx8/1Mx16]CMOS SINGLE VOLTAGE 3V ONLY FLASHMEMORY

FEATURES

- Extended single - supply voltage range 2.7V to 3.6V
- 2,097,152 x 8/1,048,576 x 16 switchable
- Single power supply operation
 - 3.0V only operation for read, erase and program operation
- **Fully compatible with MX29LV160A device**
- Fast access time: 55/70ns
- Low power consumption
 - 30mA maximum active current
 - 0.2uA typical standby current
- Command register architecture
 - Byte/word Programming (9us/11us typical)
 - Sector Erase (Sector structure 16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x31)
- Auto Erase (chip & sector) and Auto Program
 - Automatically erase any combination of sectors with Erase Suspend capability.
 - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
 - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase.
- Status Reply
 - Data polling & Toggle bit for detection of program and erase operation completion.
- Ready/Busy pin (RY/BY)
 - Provides a hardware method of detecting program or erase operation completion.
- Sector protection
 - Hardware method to disable any combination of sectors from program or erase operations
 - Temporary sector unprotect allows code changes in previously locked sectors.
- CFI (Common Flash Interface) compliant
 - Flash device parameters stored on the device and provide the host system to access
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Sector Architecture
 - T = Top Boot Sector
 - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 1.4V
- Package type:
 - 44-pin SOP
 - 48-pin TSOP
 - 48-ball CSP
- Compatibility with JEDEC standard
 - Pinout and software compatible with single-power supply Flash

GENERAL DESCRIPTION

The MX29LV160BT/BB is a 16-mega bit Flash memory organized as 2M bytes of 8 bits or 1M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV160BT/BB is packaged in 44-pin SOP, 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV160BT/BB offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV160BT/BB has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV160BT/BB uses a command register to manage this functionality. The command register allows for

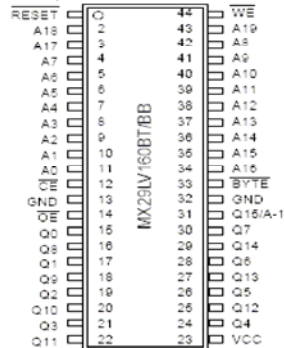
100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV160BT/BB uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE	Chip Enable Input
WE	Write Enable Input
BYTE	Word/Byte Selection input
RESET	Hardware Reset Pin/Sector Protect Unlock
OE	Output Enable Input
RY/BY	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

48 TSOP (Standard Type) (12mm x 20mm)



DC CHARACTERISTICS TA = -40°C TO 85°C, VCC = 2.7V~3.6V

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			± 1	μA	$V_{\text{IN}} = V_{\text{SS}}$ to V_{CC} , $V_{\text{CC}}=V_{\text{CC max}}$
ILIT	A9 Input Leakage Current			35	μA	$V_{\text{CC}}=V_{\text{CC max}}$; A9=12.5V
ILO	Output Leakage Current			± 1	μA	$V_{\text{OUT}} = V_{\text{SS}}$ to V_{CC} , $V_{\text{CC}}=V_{\text{CC max}}$
ICC1	VCC Active Read Current		9	16	mA	$\overline{\text{CE}}=V_{\text{IL}}$, $\overline{\text{OE}}=V_{\text{IH}}$ @5MHz
			2	4	mA	(Byte Mode) @1MHz
			9	16	mA	$\overline{\text{CE}}=V_{\text{IL}}$, $\overline{\text{OE}}=V_{\text{IH}}$ @5MHz
			2	4	mA	(Word Mode) @1MHz
ICC2	VCC Active write Current		20	30	mA	$\overline{\text{CE}}=V_{\text{IL}}$, $\overline{\text{OE}}=V_{\text{IH}}$, $\overline{\text{WE}}=V_{\text{IL}}$
ICC3	VCC Standby Current		0.2	5	μA	$\overline{\text{CE}}$; $\overline{\text{RESET}}=V_{\text{CC}} \pm 0.3\text{V}$
ICC4	VCC Standby Current During Reset (See Conditions)		0.2	5	μA	$\overline{\text{RESET}}=V_{\text{SS}} \pm 0.3\text{V}$
ICC5	Automatic sleep mode		0.2	5	μA	$V_{\text{IH}}=V_{\text{CC}} \pm 0.3\text{V}$; $V_{\text{IL}}=V_{\text{SS}} \pm 0.3\text{V}$
VIL	Input Low Voltage (Note 1)	-0.5		0.8	V	
VIH	Input High Voltage	$0.7 \times V_{\text{CC}}$		$V_{\text{CC}} + 0.3$	V	
VID	Voltage for Automatic Select and Temporary Sector Unprotect	11.5		12.5	V	$V_{\text{CC}}=3.3\text{V}$
VOL	Output Low Voltage			0.45	V	$I_{\text{OL}} = 4.0\text{mA}$, $V_{\text{CC}}=V_{\text{CC min}}$
VOH1	Output High Voltage (TTL)	$0.85 \times V_{\text{CC}}$				$I_{\text{OH}} = -2\text{mA}$, $V_{\text{CC}}=V_{\text{CC min}}$
VOH2	Output High Voltage (CMOS)	$V_{\text{CC}}-0.4$				$I_{\text{OH}} = -100\mu\text{A}$, $V_{\text{CC min}}$
VLKO	Low VCC Lock-out Voltage	1.4		2.1	V	

NOTES:

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = $V_{\text{CC}} + 1.5\text{V}$ for pulse width is equal to or less than 20 ns
If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for $t_{\text{ACC}} + 30\text{ns}$.

8. [AT24C16](#)

2-Wire Serial CMOS E²PROM 16k (2048 x 8)

The AT24C16 provides 16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V(4.5V to 5.5V), 2.7V(2.7V to 5.5V) and 1.8V(1.8V to 5.5V) versions.

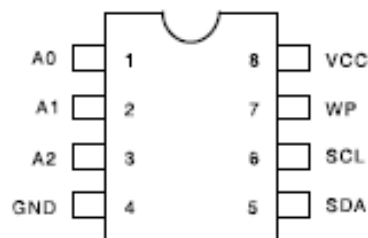
Features

- Low Voltage and Standard Voltage Operation
 - 5.0 (V_{CC} = 4.5V to 5.5V)
 - 2.7 (V_{CC} = 2.7V to 5.5V)
 - 2.5 (V_{CC} = 2.5V to 5.5V)
 - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
 - Endurance: 1 Million Cycles
 - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages

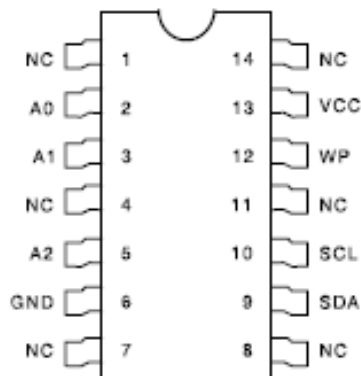
Pin Configurations

Pin Name	Function
A ₀ to A ₂	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

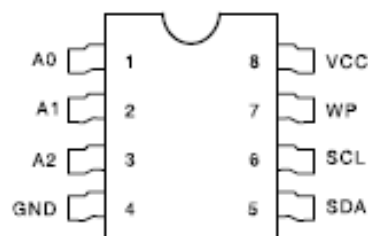
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



Pin Capacitance ⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current $V_{CC} = 5.0\text{V}$	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current $V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		0.6	3.0	μA
I_{SB2}	Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.4	4.0	μA
I_{SB3}	Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.6	4.0	μA
I_{SB4}	Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		8.0	18.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾		-1.0		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾			$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $C_L = 1$ TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
fSCL	Clock Frequency, SCL		100		400	kHz
tLOW	Clock Pulse Width Low	4.7		1.2		μs
tHIGH	Clock Pulse Width High	4.0		0.6		μs
tI	Noise Suppression Time ⁽¹⁾		100		50	ns
tAA	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	μs
tBUF	Time the bus must be free before a new transmission can start ⁽¹⁾	4.7		1.2		μs
tHD.STA	Start Hold Time	4.0		0.6		μs
tSU.STA	Start Set-up Time	4.7		0.6		μs
tHD.DAT	Data In Hold Time	0		0		μs
tSU.DAT	Data In Set-up Time	200		100		ns
tR	Inputs Rise Time ⁽¹⁾		1.0		0.3	μs
tF	Inputs Fall Time ⁽¹⁾		300		300	ns
tSU.STO	Stop Set-up Time	4.7		0.6		μs
tDH	Data Out Hold Time	100		50		ns
tWR	Write Cycle Time		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

9. [NJM4558](#) DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

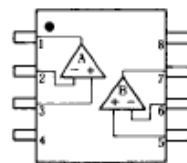
The NJM4558/4559 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

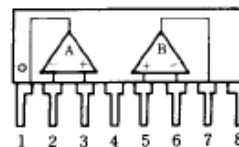
■ FEATURES

- Operating Voltage ($\pm 4V \sim \pm 18V$)
- High Voltage Gain (100dB typ.)
- High Input Resistance ($5M\Omega$ typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM4558D, NJM4558M, NJM4558V
NJM4559D, NJM4559M, NJM4559V



NJM4558L
NJM4559L

PIN FUNCTION

1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. V⁻
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8. V⁺

■ ELECTRICAL CHARACTERISTICS

($V^+V^- = \pm 15V, T_a = 25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	$R_s \leq 10k\Omega$	-	0.5	6	mV
Input Offset Current	I_{IO}		-	5	200	nA
Input Bias Current	I_B		-	25	500	nA
Input Resistance	R_{IN}		0.3	5	-	$M\Omega$
Large Signal Voltage Gain	A_V	$R_L \geq 2k\Omega, V_O = \pm 10V$	86	100	-	dB
Maximum Output Voltage Swing 1	V_{OM1}	$R_L \geq 10k\Omega$	± 12	± 14	-	V
Maximum Output Voltage Swing 2	V_{OM2}	$R_L \geq 2k\Omega$	± 10	± 13	-	V
Input Common Mode Voltage Range	V_{ICM}		± 12	14	-	V
Common Mode Rejection Ratio	CMR	$R_s \leq 10k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVR	$R_s \leq 10k\Omega$	76.5	90	-	dB
Operating Current	I_{CC}		-	3.5	5.7	mA
Slew Rate						
NJM4558	SR		-	1	-	V/ μs
NJM4559	SR		-	2	-	V/ μs
Equivalent Input Noise Voltage	V_{NI}	$R_{IAA}, R_s = 2.2k\Omega, 30kHz$ LPF	-	1.4	-	μV_{rms}
Gain Bandwidth Product	GB					
NJM4558				3		MHz
NJM4559				6		MHz

10. [WM8714](#) 24-bit, 96kHz Stereo DAC

The WM8714 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8714 supports data input word lengths from 16 to 24-bits and sampling rates up to 96kHz. The WM8714 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-pin SOIC package.

The WM8714 has a hardware control interface for selection of audio data interface format, mute and de-emphasis. The WM8714 supports I²S, and right Justified audio data interfaces.

The WM8714 is an ideal device to interface to AC-3TM, DTSTM, and MPEG audio decoders for surround sound applications, or for use in DVD players.

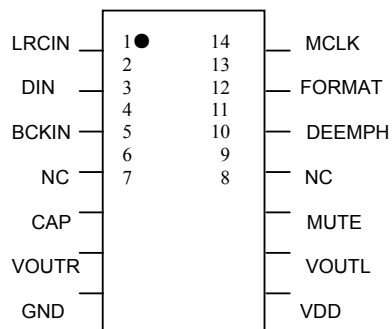
• FEATURES

- Stereo DAC
- Audio Performance
 - 95dB SNR ('A' weighted @ 48kHz) DAC

Boxes

- -90dB THD
- DAC Sampling Frequency: 8kHz – 96kHz
- Pin Selectable Audio Data Interface Format
 - I²S, Right Justified or DSP
- 3-5V Supply Operation
- 14-pin SOIC Package
- Pin Compatible with WM8725

• Pin Configuration



• APPLICATIONS

- DVD Players
- Digital TV
- Digital Set Top

• Pin Description

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCKIN	Digital input	Bit clock input
4	NC	No connect	No internal connection
5	CAP	Analogue output	Analogue internal reference
6	VOUTR	Analogue output	Right channel DAC output
7	GND	Supply	Negative supply
8	VDD	Supply	Positive supply
9	VOUTL	Analogue output	Left channel DAC output
10	MUTE	Digital input	Soft mute control, Internal pull down High = Mute ON Low = Mute OFF
11	NC	No connect	No internal connection
12	DEEMPH	Digital input	De-emphasis select, Internal pull up High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified High = 16-24-bit I ² S
14	MCLK	Digital input	System clock input

ICS ON HI-VOLTAGE BOARD

1. [BIT3193](#) High Performance PWM Controller

BIT3193 integrated circuit provides the essential features for general purpose PWM controller in a small low cost 16-pin package. BIT3193 has built-in a low frequency PWM generator for any specified application. BIT3193 includes latched off protection feature may make the system more reliable while compare to other similar products.

• Features

- 4.5V ~ 8V operation
- Fixed High Frequency, Voltage Mode PWM Control
- Latched Off Protection
- Build-In Low Frequency PWM Generator
- Build-in UVLO
- Low Power CMOS Process
- Totem Pole Output
- 16 Pin Package

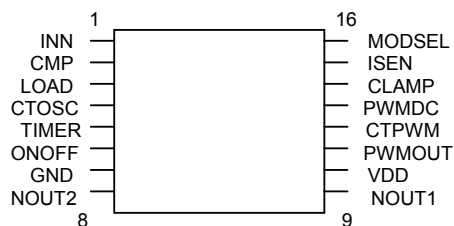
• Applications

- DC/DC Converters
- LCD TV
- LCD Monitor
- Notebook Computer
- Tablet PC
- Personal Digital Assistants
- Navigation Phone/ Door Phone
- Portable consumer product

• Recommended Operating Condition:

Supply Voltage	4.5~8V
Operating Ambient Temperature	0~70 ° C
Operating Frequency	50K~400K Hz

• Pin Layout:

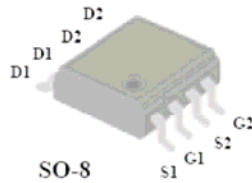


• Pin Description

Pin No.	Symbol	I/O	Descriptions
1	INN	I/O	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	LOAD	I/O	A switch that connected to the high frequency triangle wave generator. This switch is open while ISEN pin <1.3V. An external resistor connected here may change the operation frequency of CTOSC in open load situation.
4	CTOSC	I/O	An external capacitor connected here can set the frequency of high frequency PWM controller.
5	TIMER	I/O	With internal reference current and an external capacitor connected here can set the required period of starting and the timing of initialization. The controller is forced to reset mode while TIMER<0.3V. During reset mode, a~60uA current will flow into the INN pin to reduce the output level of the error amplifier CMP to turn off the controller. The latched off protection function will be enable after this node is charged to>2.5V. System is latched off if any abnormal operation is detected if pin TIMER>2.5V. The output current of this pin is 20uA when TIMER<0.3V. The output current becomes to 1uA when TIMER>0.3V.
6	ONOFF	I	The control pin of turning on or off the IC.1V threshold with an internal 80K $\pm$ 15% ohm pull-low resistor.
7	GND	I/O	The ground pin of the device.
8	NOUT2	O	The number 2 output driver for driving the NMOSFET switch.
9	NOUT1	O	The number 1 output driver for driving the NMOSFET switch.
10	VDD	I	The power supplies pin of the device.
11	PWMOUT	O	The output pin of low frequency PWM generator. A 2.5V or floating two state output is provided through this pin. The internal circuit limits the max. Duty-cycle to ~92%.
12	CTPWM	I/O	With the internal reference current and an external capacitor connected here can set the operation frequency of low frequency PWM generator with 1.0V~2.5V triangle wave output.
13	PWMDC	I	Low frequency PWM controlling input. A PWM output comes out by comparing this DC input and the 1.0~2.5V triangle wave that is generated by CTPWM.
14	CLAMP	I	Over voltage clamping. If a>2.0V voltage is detected. A~60uA current will flow into the INN pin to reduce the output of the error amplifier pin CMP to regulate the output voltage.
15	ISEN	I	Load current detection pin, the open load situation is detected if a less than 1.3V input is sensed.
16	MODSEL	O	To set the output polarity of the low frequency PWM controller.

2. [AP4511M](#) N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Performance

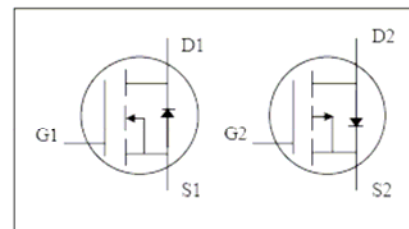


N-CH	BV_{DSS}	35V
	$R_{DS(ON)}$	25m Ω
	I_D	7A
P-CH	BV_{DSS}	-35V
	$R_{DS(ON)}$	40m Ω
	I_D	-6.1A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	35	-35	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current ³	7	-6.1	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current ³	5.7	-5	A
I_{DM}	Pulsed Drain Current ¹	30	-30	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ\text{C}/\text{W}$

Part 3 Detailed Circuit

MAIN BOARD

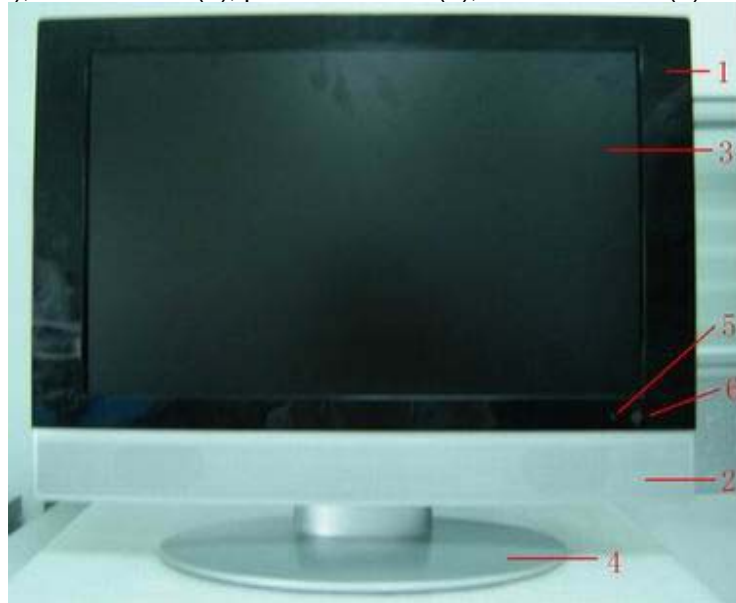
DVD BOARD

HI-VOLTAGE BOAD

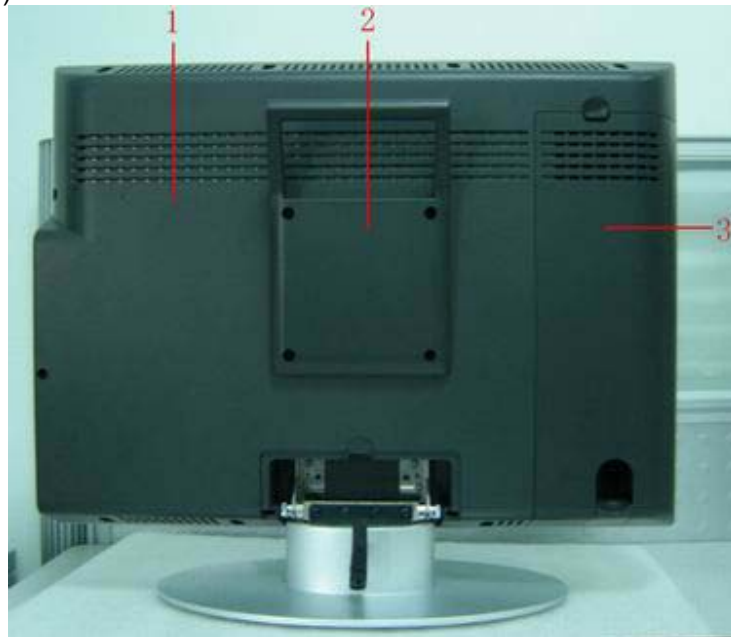
VGA BOAD

Part 4 Disassemble/Assemble Procedure

1. Fig1: Front view of the whole assembly diagram in which: front panel (1), middle panel (2), LCD screen (3), base bottom (4), power indicator (5), remote sensor (6).



2. Fig2: Back view of the whole assembly diagram in which: rear panel (1), handle (2), cover for lines output (3).



3. Fig3: Back view without handle and cover for lines output. Remove four screws from (A) position.

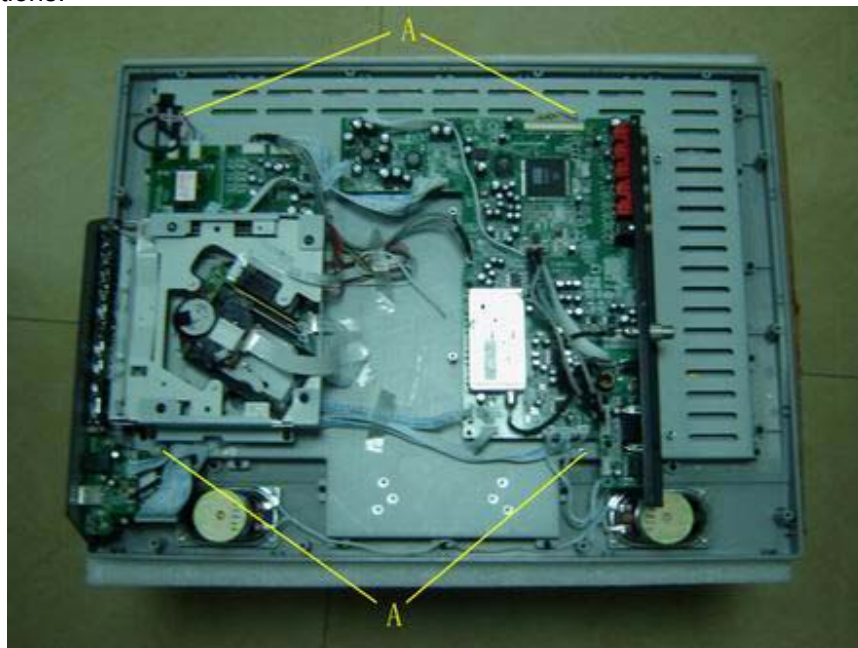


4. Fig4: Assembly diagram without the rear panel and base bottom in which: shield cover (1), side panel (2), key pad (3), right shield panel (4), LCD shield (5), speaker (6).

Remove the screws for rear panel fixing from positions like (A). Remove the screws for base bottom fixing from (B) position.

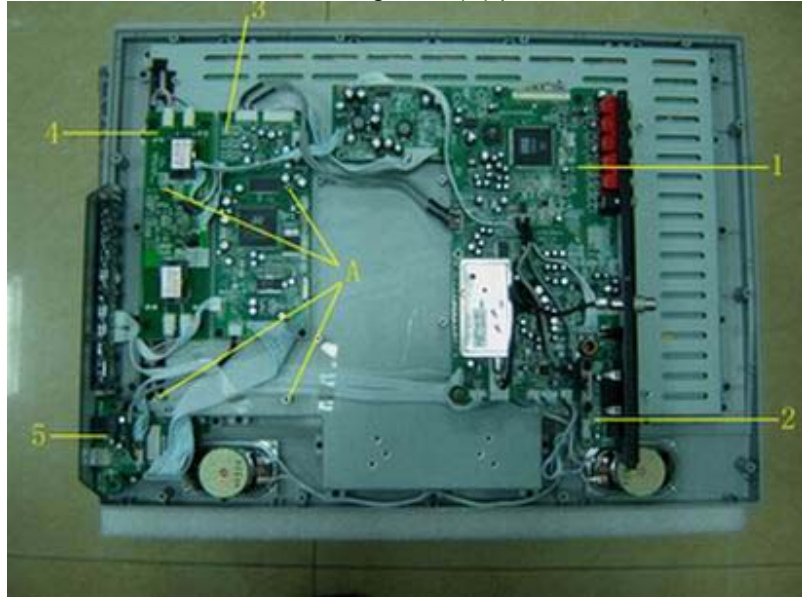


5. Fig5: Assembly diagram without shield cover. Remove the screws for shield cover fixing from (A) positions.

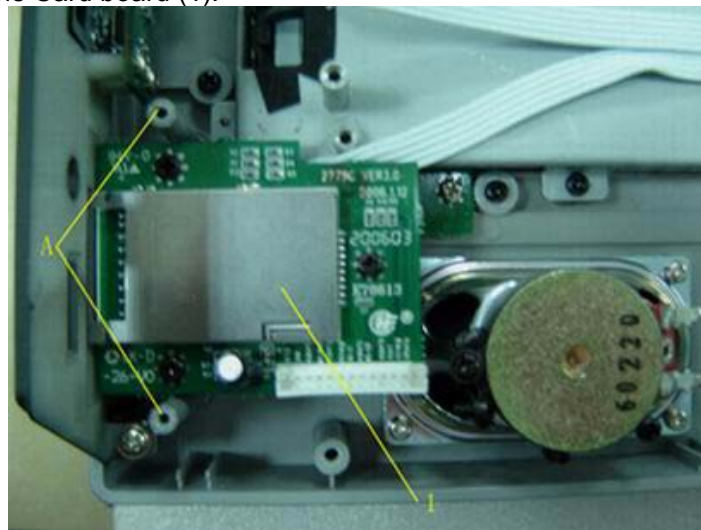


6. Fig6: Assembly diagram without DVD loader in which: Main board (1), VGA board (2), DVD board (3), HI-voltage board (4), Eadphone board (5).

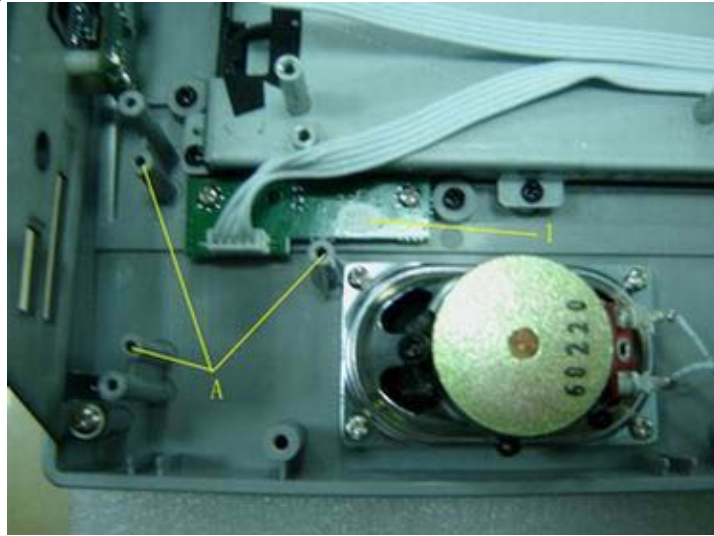
Remove the screws for loader fixing from (A) position.



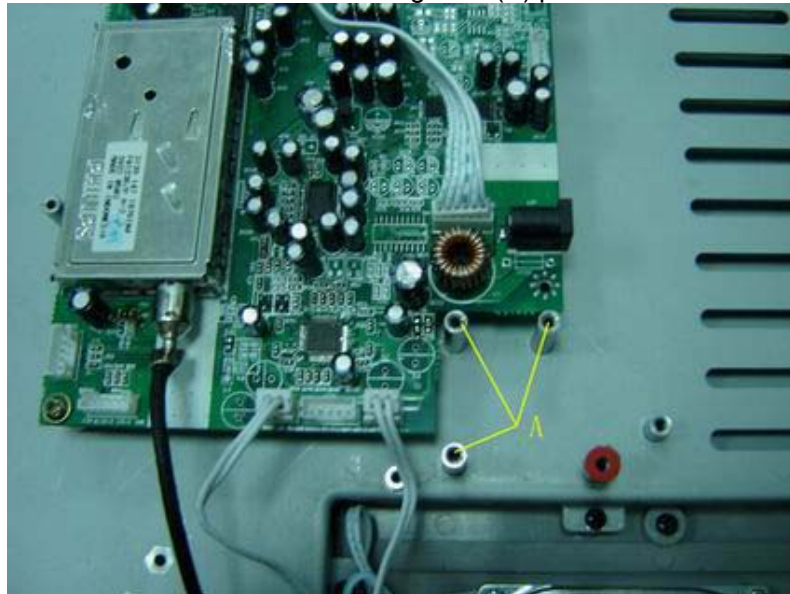
7. Fig7: Remove the USB and headphone board and the screws for its fixing from (A) positions to see the Card board (1).



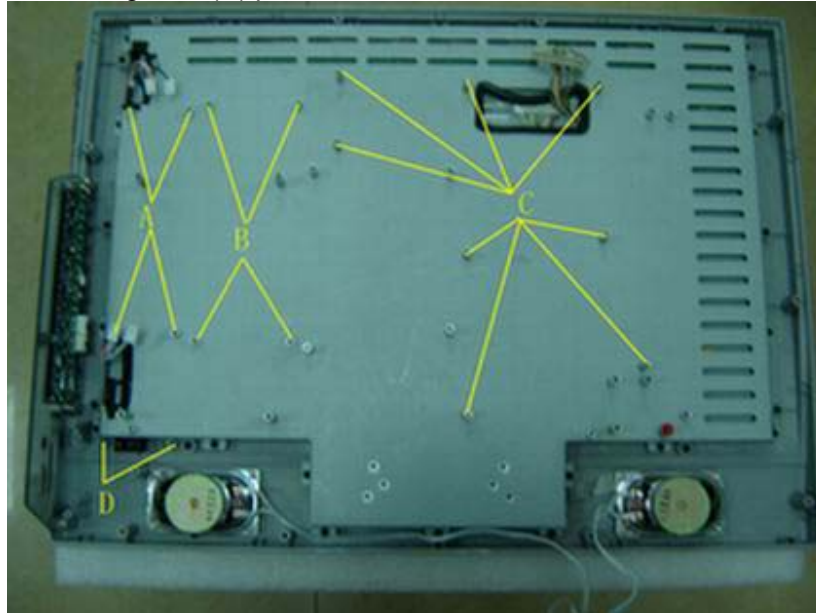
8. Fig8: Remove the screws for Card board fixing from (A) positions to see the Remote control board (1).



9. Fig9: Remove the screws for VGA board fixing from (A) positions.



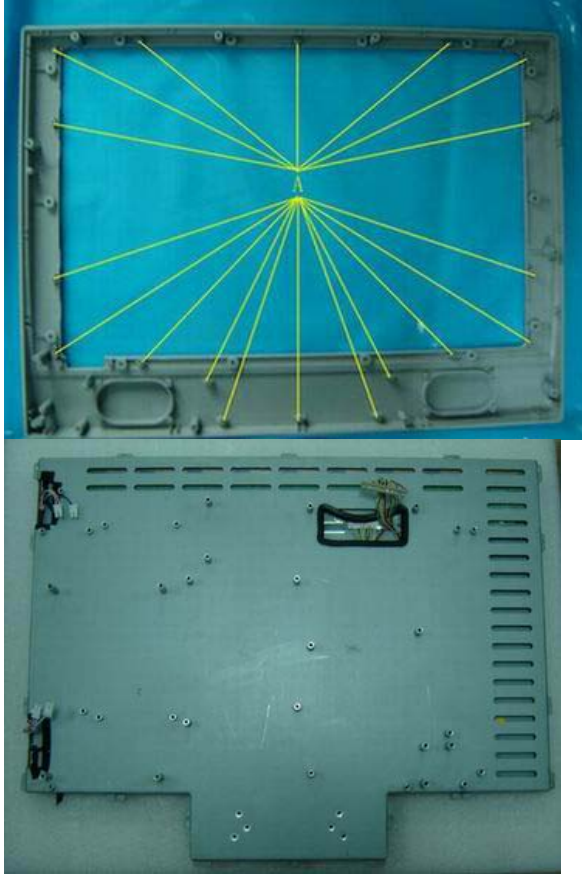
10. Fig10: Remove the screws for HI-voltage fixing from (A) positions, screws for DVD board fixing from (B) positions, screws for main board fixing from (C) positions and screws for remote control board fixing from (D) positions.



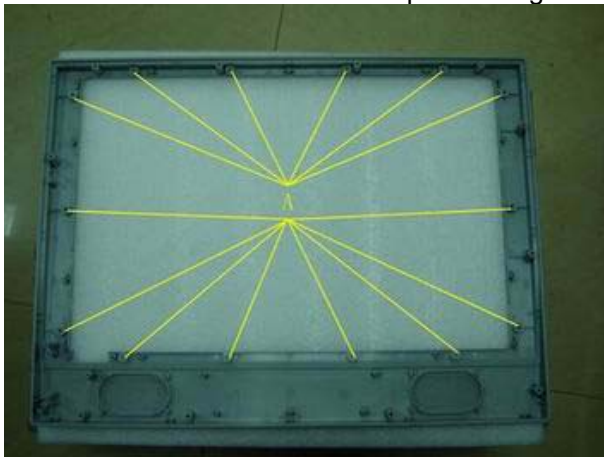
11. Fig11: Remove the screws for side panel fixing from (A) positions and screws for speakers fixing from (B) positions.



13. Fig13: Remove the screws for LCD screen and its shield fixing from (A) positions.



14. Fig14: Back view of the middle panel and front view of the front panel. Remove the screws for front panel fixing from (A) positions.





15. Fig15: The connections between the DVD board and the Card board, the USB and Headphone board, the Key pad board.

